Memory FeRAM

1M (128 K × 8) Bit SPI

MB85RS1MT

■ DESCRIPTION

MB85RS1MT is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 131,072 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85RS1MT adopts the Serial Peripheral Interface (SPI).
The MB85RS1MT is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85RS1MT can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
MB85RS1MT does not take long time to write data like Flash memories or E^2PROM, and MB85RS1MT takes no wait time.

■ FEATURES

- Bit configuration : 131,072 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 1.8 V to 2.7 V, 25 MHz (Max)
  2.7 V to 3.6 V, 30 MHz (Max)
  For FSTRD command 2.7 V to 3.6 V, 40 MHz (Max)
- High endurance : 10^{13} times / byte
- Data retention : 10 years (+85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power consumption : Operating power supply current 9.5 mA (Max@30 MHz)
  Standby current 120 μA (Max)
  Sleep current 10 μA (Max)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 8-pin plastic SOP 150mil
  8-pin plastic DFN 5mm × 6mm
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited.
RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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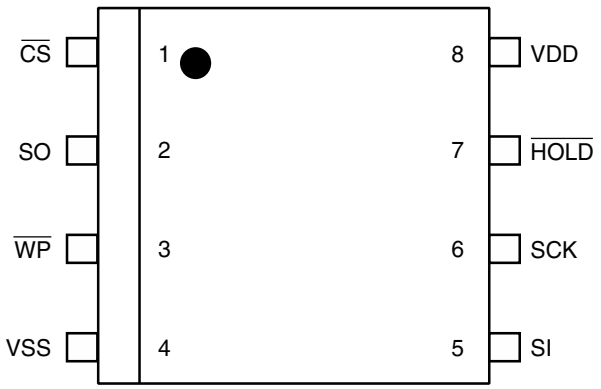
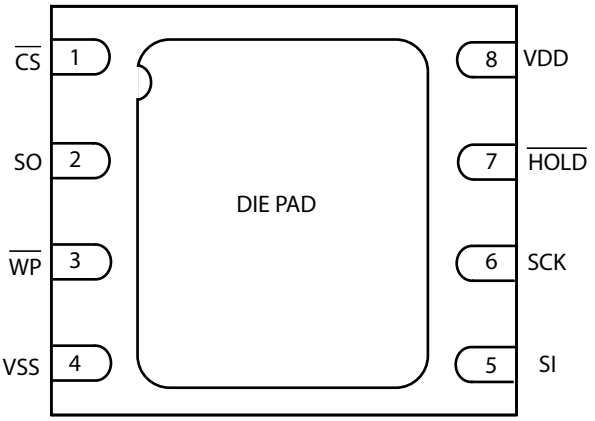
■ PIN ASSIGNMENT

(TOP VIEW)



(8-pin plastic SOP 150mil)

(TOP VIEW)

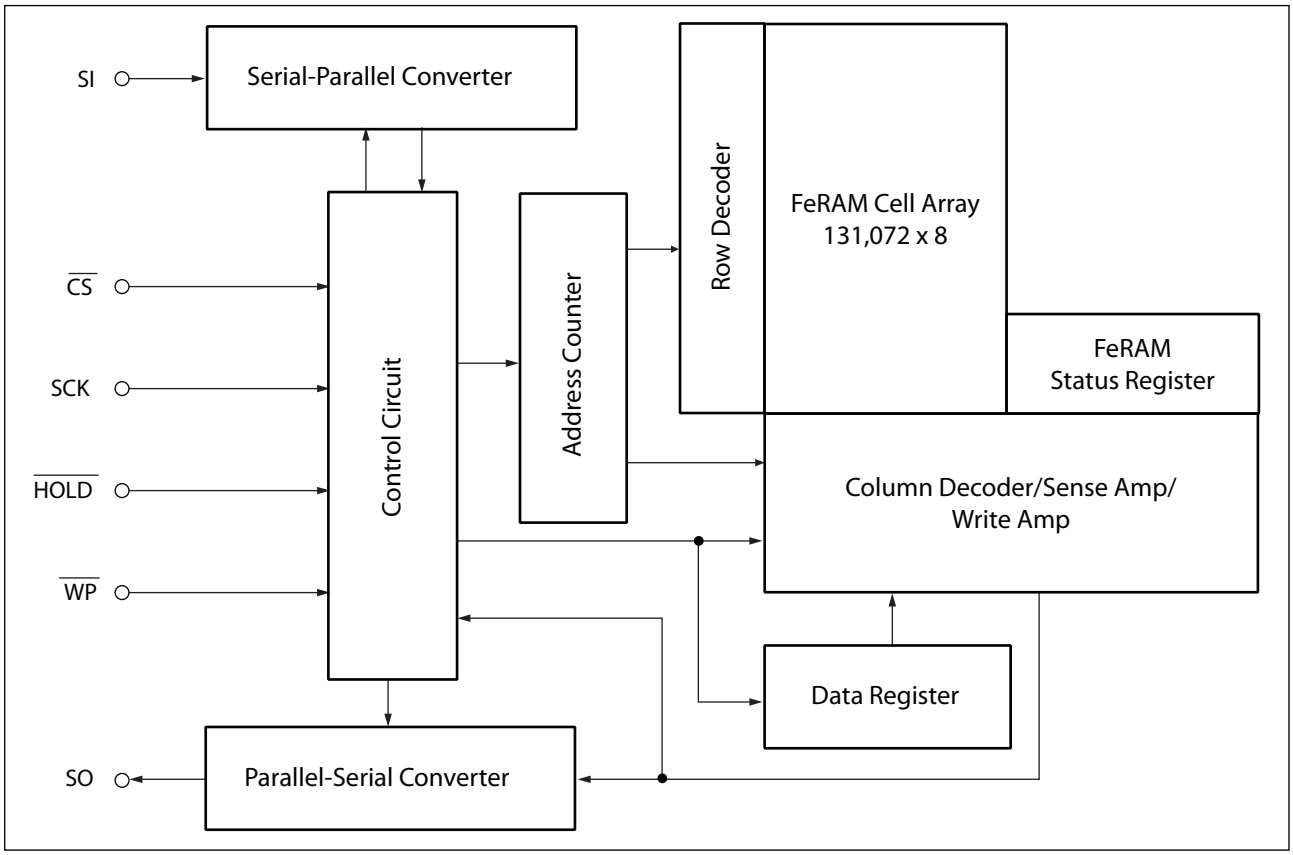


(8-pin plastic DFN 5mm × 6mm)

■ PIN FUNCTIONAL DESCRIPTIONS

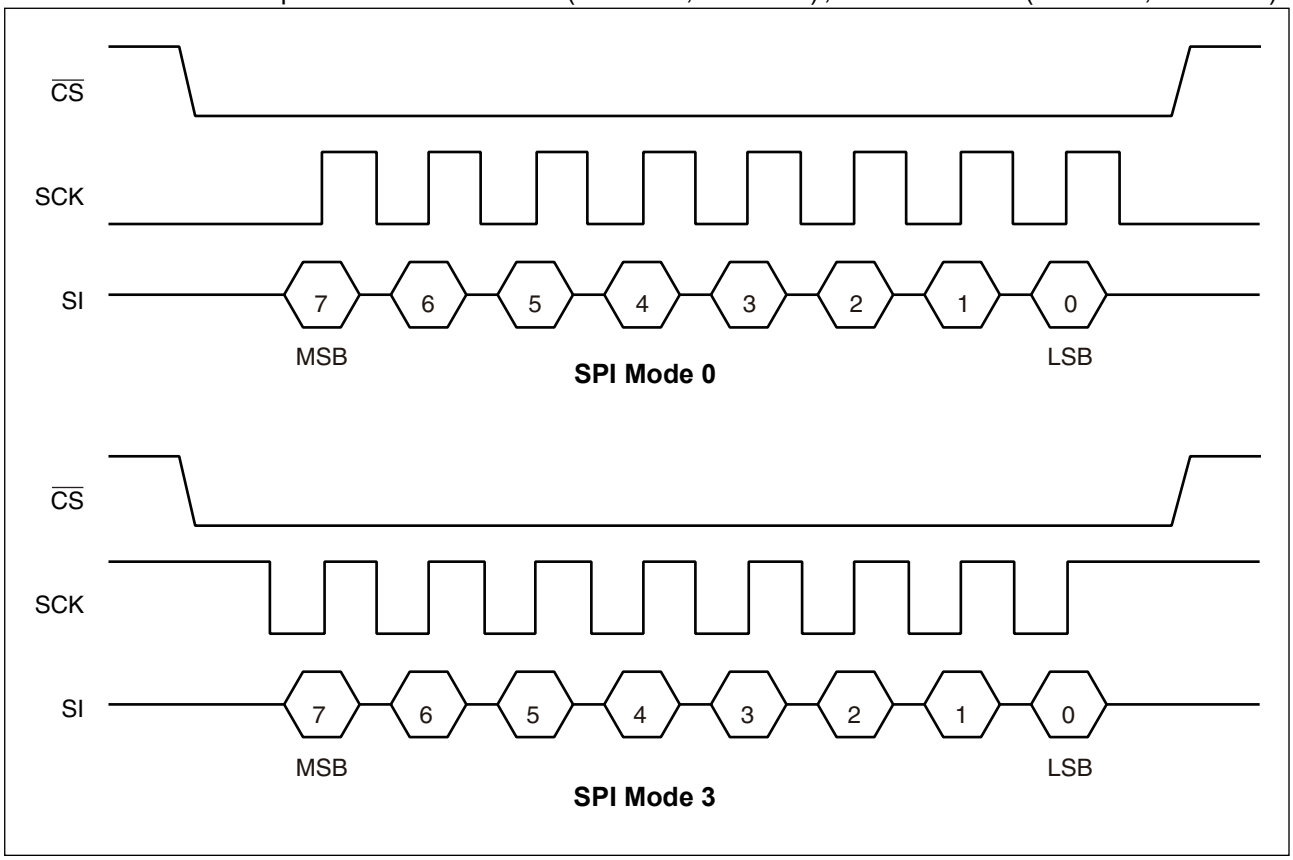
Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is “L” level, device is in select (active) status. $\overline{CS}$ has to be “L” level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in related with $\overline{WP}$ and WPEN. See “ ■WRITING PROTECT” for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is “L” level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See “■ HOLD OPERATION” for detail.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin
DIE PAD	—	It is allowed for the DIE PAD on the bottom of the DFN8 package to be floating (no connection to anything) or to be connected to VSS.

■ BLOCK DIAGRAM



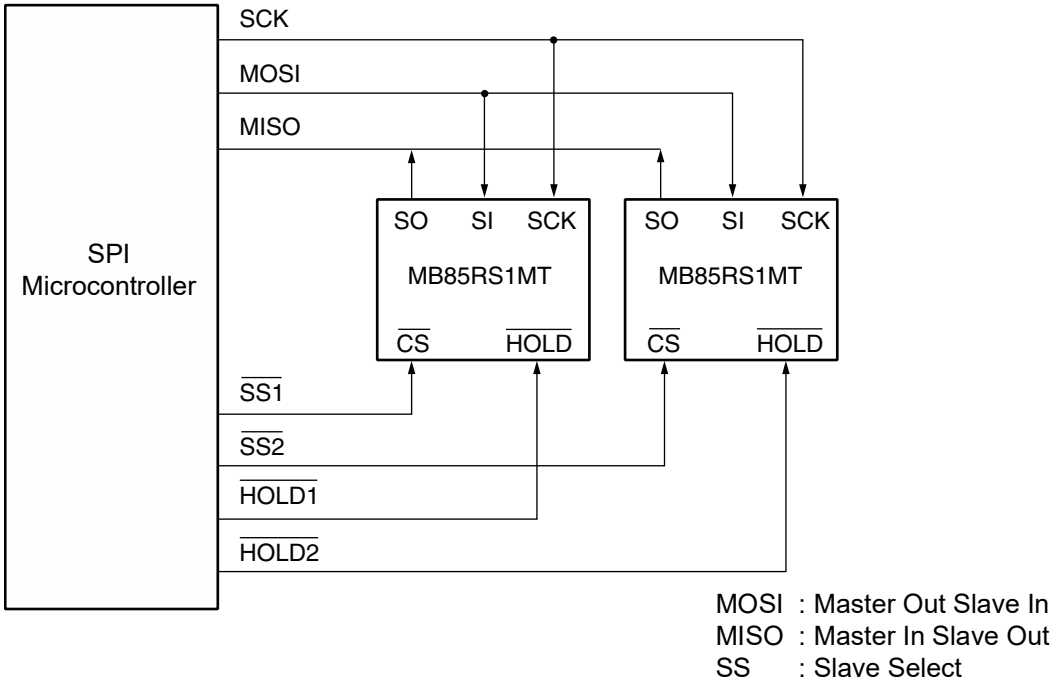
■ SPI MODE

MB85RS1MT corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .

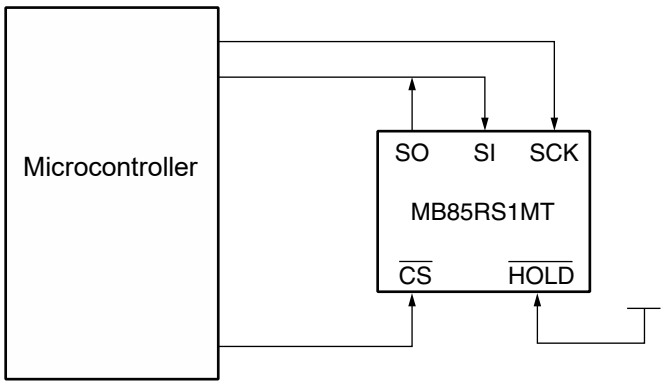


■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS1MT works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to " ■WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to " ■BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. The rising edge of $\overline{CS}$ after WRSR command recognition. The rising edge of $\overline{CS}$ after WRITE command recognition. After return from SLEEP mode.
0	0	This is a bit fixed to "0".

■ OP-CODE

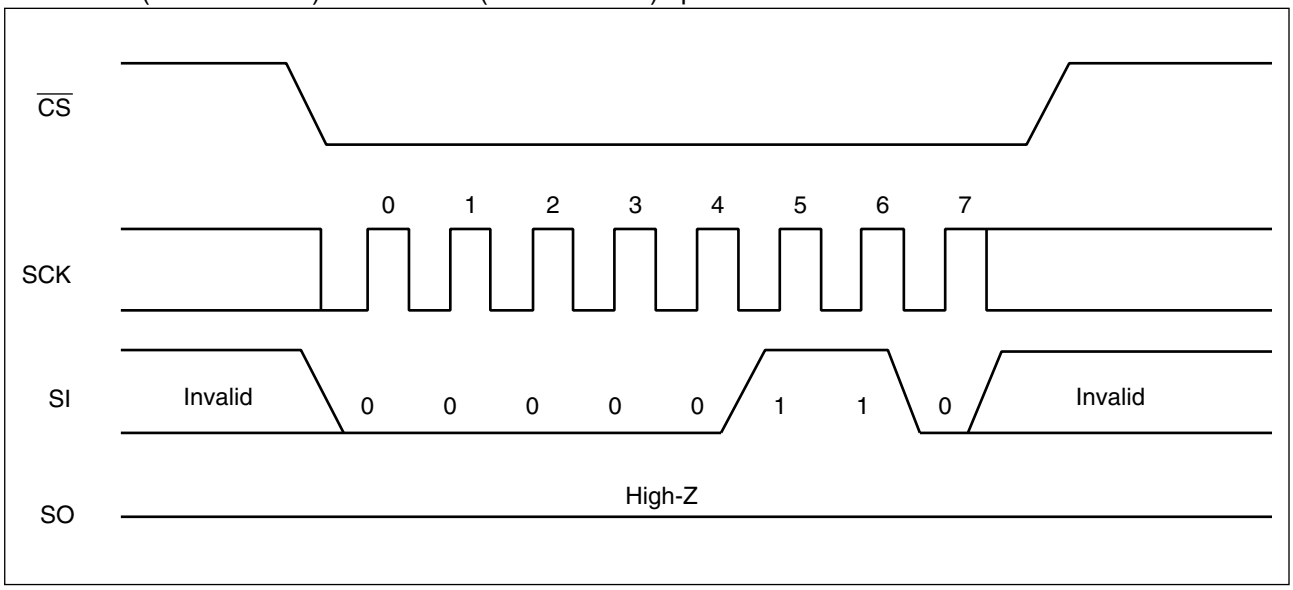
MB85RS1MT accepts 9 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	$0000\ 0110_B$
WRDI	Reset Write Enable Latch	$0000\ 0100_B$
RDSR	Read Status Register	$0000\ 0101_B$
WRSR	Write Status Register	$0000\ 0001_B$
READ	Read Memory Code	$0000\ 0011_B$
WRITE	Write Memory Code	$0000\ 0010_B$
RDID	Read Device ID	$1001\ 1111_B$
FSTRD	Fast Read Memory Code	$0000\ 1011_B$
SLEEP	Sleep Mode	$1011\ 1001_B$

■ COMMAND

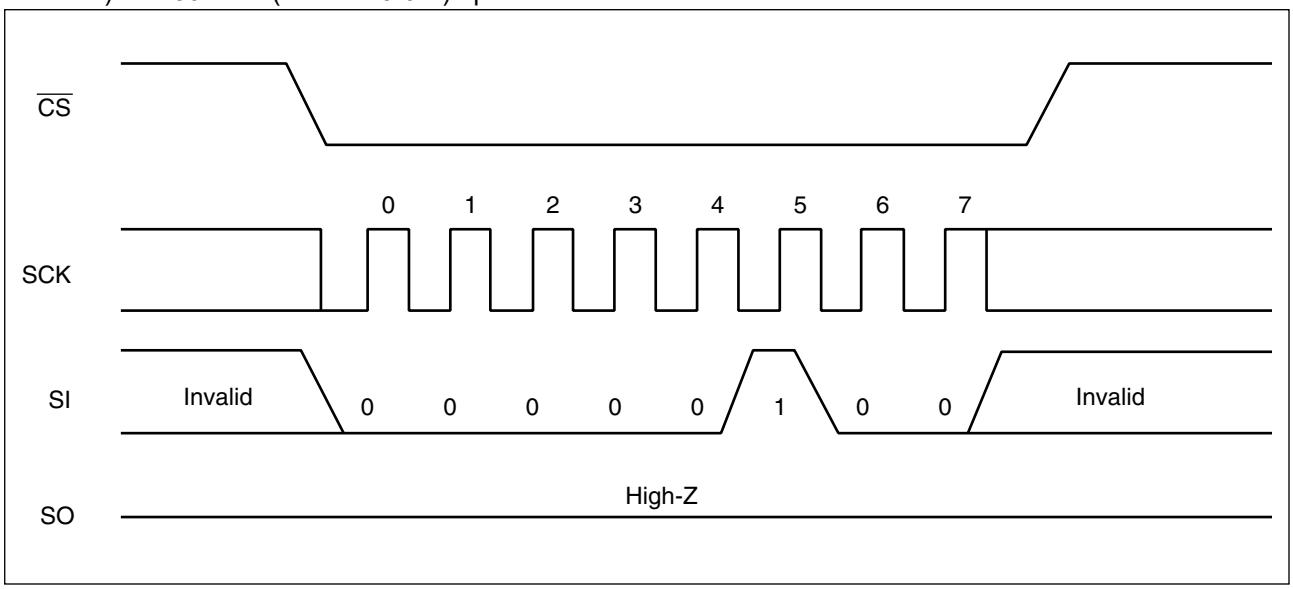
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) . WREN command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



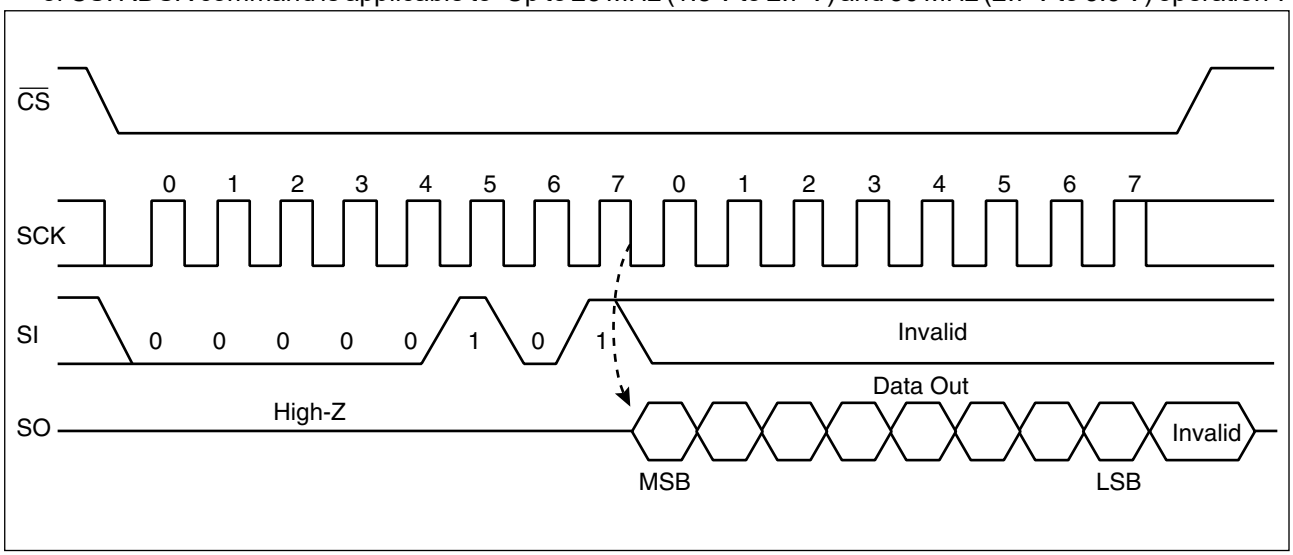
• WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset. WRDI command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



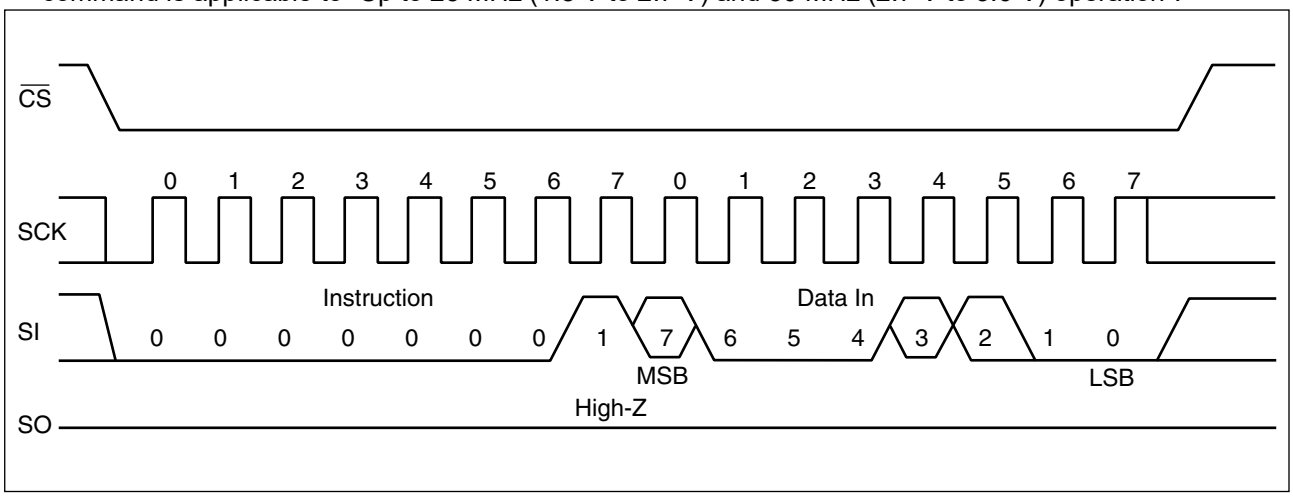
• **RDSR**

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$. RDSR command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



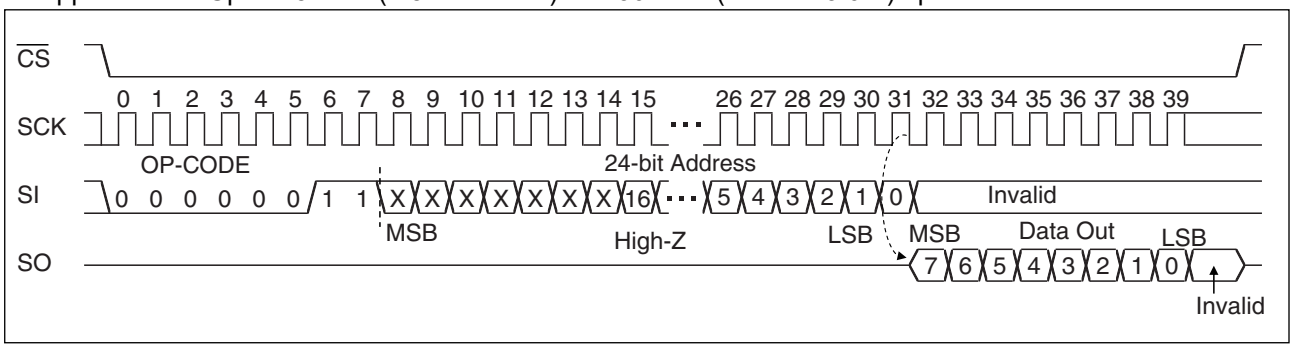
• **WRSR**

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{WP}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence. WRSR command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



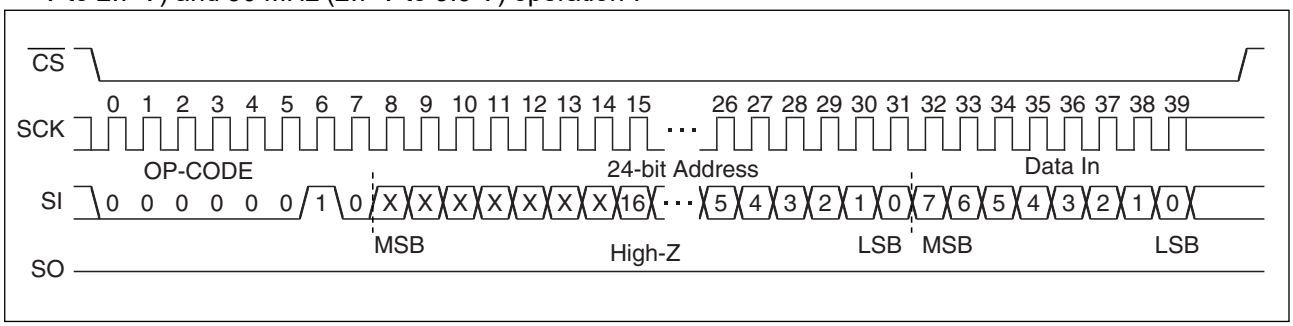
• **READ**

The READ command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 7-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. READ command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



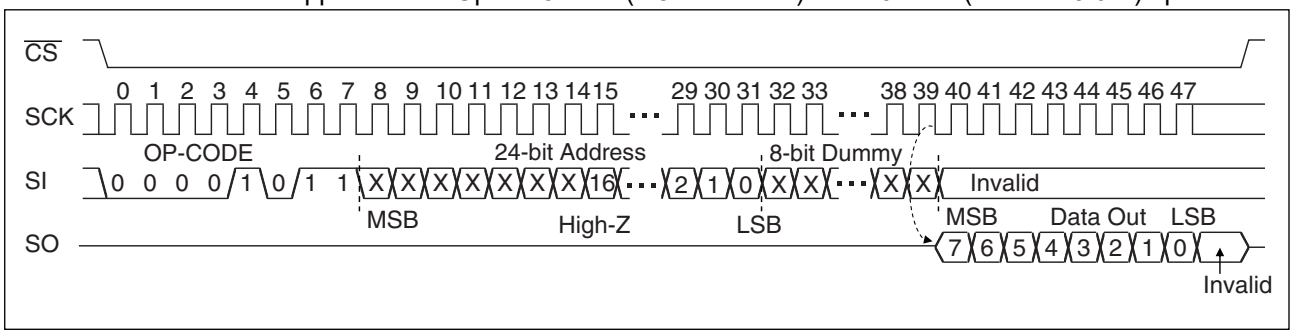
• **WRITE**

The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 7-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely. WRITE command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



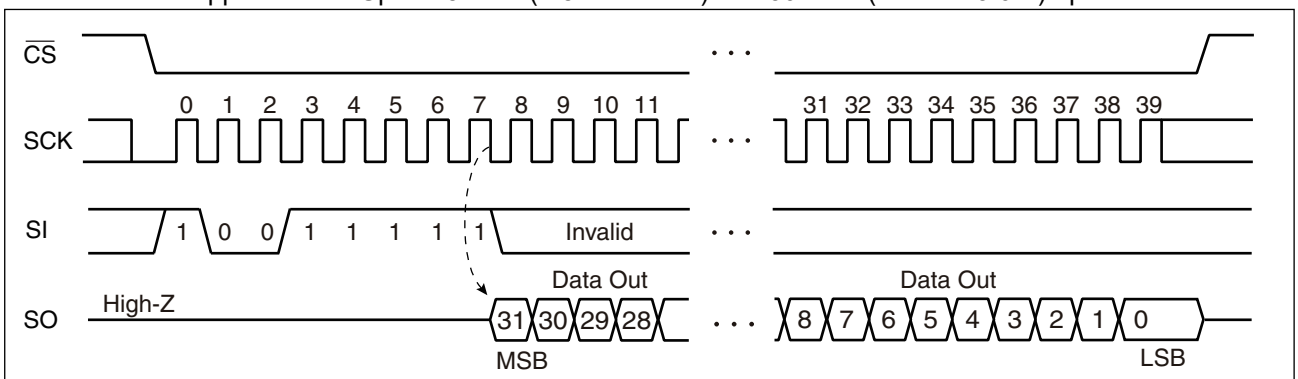
- **FSTRD**

The FSTRD command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 7-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely. FSTRD command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 40 MHz (2.7 V to 3.6 V) operation”.



- **RDID**

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen. RDID command is applicable to “Up to 25 MHz (1.8 V to 2.7 V) and 30 MHz (2.7 V to 3.6 V) operation”.



	bit									
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Hex**	
Manufacturer ID	0	0	0	0	0	1	0	0	04_H	RAMXEED
Continuation code	0	1	1	1	1	1	1	1	$7F_H$	

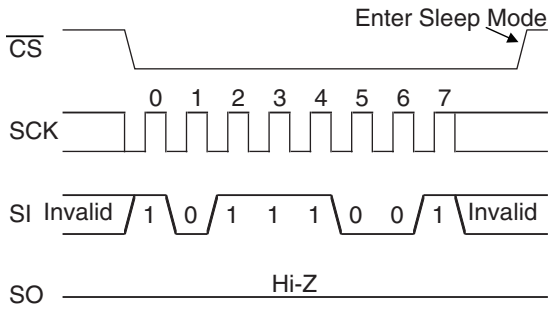
	Proprietary use			Density					Hex	
Product ID (1st Byte)	0	0	1	0	0	1	1	1	27_H	Density: 00111_B = 1 Mbit

	Proprietary use								Hex	
Product ID (2nd Byte)	0	0	0	0	0	0	1	1	03_H	

• **SLEEP**

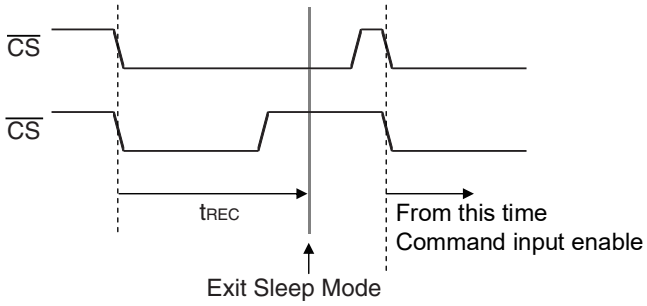
The SLEEP command shifts the LSI to a low power mode called “SLEEP mode”. The transition to the SLEEP mode is carried out at the rising edge of $\overline{CS}$ after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are logically ignored and SO changes to a Hi-Z state. If input pin(s) other than $\overline{CS}$ pin is (are) not fixed to VSS or VDD, flow-throw current may flow.



Sleep Mode Entry

Returning to an normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μs) time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before t_{REC} time. However, it is prohibited to bring down $\overline{CS}$ to L level again during t_{REC} period.



Sleep Mode Exit

■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	18000_H to $1FFFF_H$ (upper 1/4)
1	0	10000_H to $1FFFF_H$ (upper 1/2)
1	1	00000_H to $1FFFF_H$ (all)

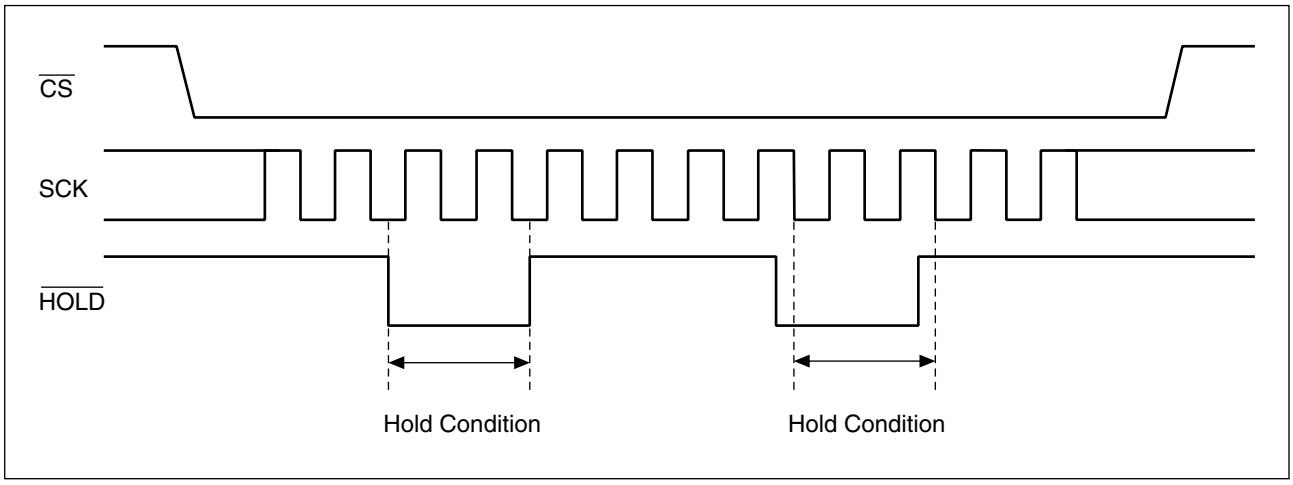
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{HOLD}$ is “L” level while $\overline{CS}$ is “L” level. The timing for starting and ending hold status depends on the SCK to be “H” level or “L” level when a $\overline{HOLD}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{HOLD}$ pin transited to “L” level when SCK is “L” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “L” level. In the same manner, in case the $\overline{HOLD}$ pin transited to “L” level when SCK is “H” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “H” level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{CS}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_{IN}	− 0.5	V_{DD} + 0.5(≤ 4.0V)	V
Output voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5(≤ 4.0V)	V
Operation ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 55	+ 125	°C

*: These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*1	V_{DD}	1.8	3.3	3.6	V
Operation ambient temperature*2	T_A	− 40	—	+ 85	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*1	$\|I_{LI}\|$	$0 \le \overline{CS} < V_{DD}$	—	—	200	μA
		$\overline{CS} = V_{DD}$	—	—	1	
		$\overline{WP}$, $\overline{HOLD}$, SCK SI = 0 V to V_{DD}	—	—	1	
Output leakage current*2	$\|I_{LO}\|$	SO = 0 V to V_{DD}	—	—	1	μA
Operating power supply current	I_{DD}	SCK = 1 MHz	—	0.77	—	mA
		SCK = 10 MHz	—	2.3	—	mA
		SCK = 25 MHz	—	4.85	—	mA
		SCK = 30 MHz	—	5.7	9.5	mA
Standby current	I_{SB}	SCK = SI = $\overline{CS}$ = V_{DD}	—	25	120	μA
Sleep current	I_{ZZ}	$\overline{CS}$ = V_{DD} All inputs V_{SS} or V_{DD}	—	—	10	μA
Input high voltage	V_{IH}	V_{DD} = 1.8 V to 3.6 V	$V_{DD} \times 0.7$	—	$V_{DD} + 0.5$	V
Input low voltage	V_{IL}	V_{DD} = 1.8 V to 3.6 V	− 0.5	—	$V_{DD} \times 0.3$	V
Output high voltage	V_{OH}	I_{OH} = − 2 mA	V_{DD} − 0.5	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
Pull up resistance for $\overline{CS}$	R_P	—	18	33	80	kΩ

*1 : Applicable pin : $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, SCK, SI

*2 : Applicable pin : SO

2. AC Characteristics

Parameter	Symbol	Value				Unit
		Up to 25 MHz operation*1 (V_{DD} = 1.8 V to 2.7 V)		Up to 30 MHz operation*2 (V_{DD} = 2.7 V to 3.6 V)		
		Min	Max	Min	Max	
SCK clock frequency (All commands except FSTRD command)	f_{CK}	0	25	0	30	MHz
SCK clock frequency (for FSTRD command)	f_{CK}	0	25	0	40	MHz
Clock high time	t_{CH}	15	—	11	—	ns
Clock low time	t_{CL}	15	—	11	—	ns
Chip select set up time	t_{CSU}	10	—	10	—	ns
Chip select hold time	t_{CSH}	10	—	10	—	ns
Output disable time	t_{OD}	—	12	—	12	ns
Output data valid time	t_{ODV}	—	18	—	9	ns
Output hold time	t_{OH}	0	—	0	—	ns
Deselect time	t_{D}	40	—	40	—	ns
Data in rising time	t_{R}	—	50	—	50	ns
Data falling time	t_{F}	—	50	—	50	ns
Data set up time	t_{SU}	5	—	5	—	ns
Data hold time	t_{H}	5	—	5	—	ns
$\overline{\text{HOLD}}$ set uptime	t_{HS}	10	—	10	—	ns
$\overline{\text{HOLD}}$ hold time	t_{HH}	10	—	10	—	ns
$\overline{\text{HOLD}}$ output floating time	t_{HZ}	—	20	—	20	ns
$\overline{\text{HOLD}}$ output active time	t_{LZ}	—	20	—	20	ns
SLEEP recovery time	t_{REC}	—	400	—	400	µs

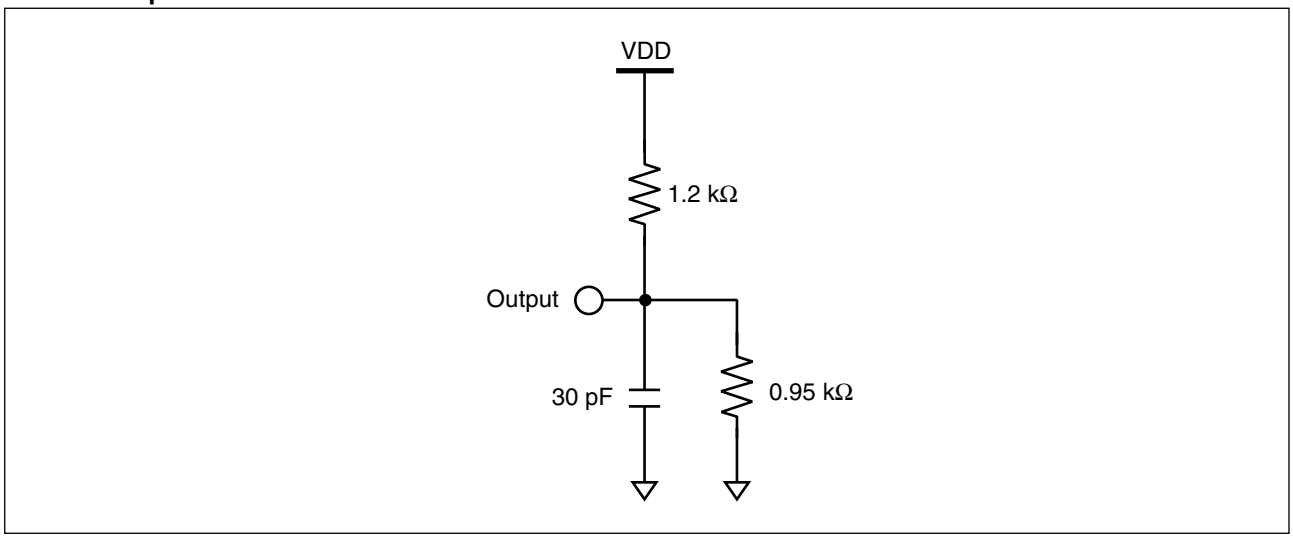
*1 : All commands except FSTRD are applicable to “Up to 25 MHz operation” in V_{DD} = 1.8 V to 2.7 V.

*2 : All commands except FSTRD are applicable to “Up to 30 MHz operation” in V_{DD} = 2.7 V to 3.6 V.

AC Test Condition

Power supply voltage : 1.8 V to 3.6 V
Operation ambient temperature : − 40 °C to + 85 °C
Input voltage magnitude : $V_{DD} \times 0.7 \leq V_{IH} \leq V_{DD}$
$0 \leq V_{IL} \leq V_{DD} \times 0.3$
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit

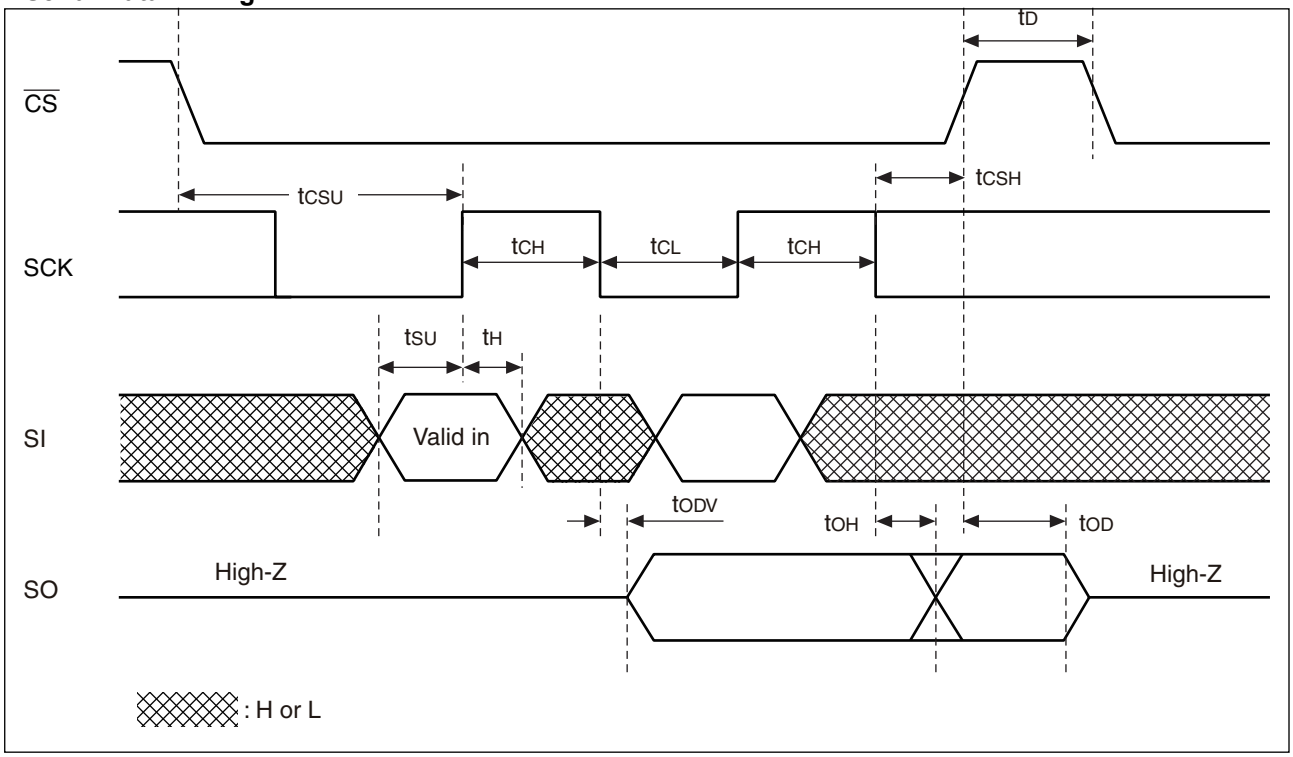


3. Pin Capacitance

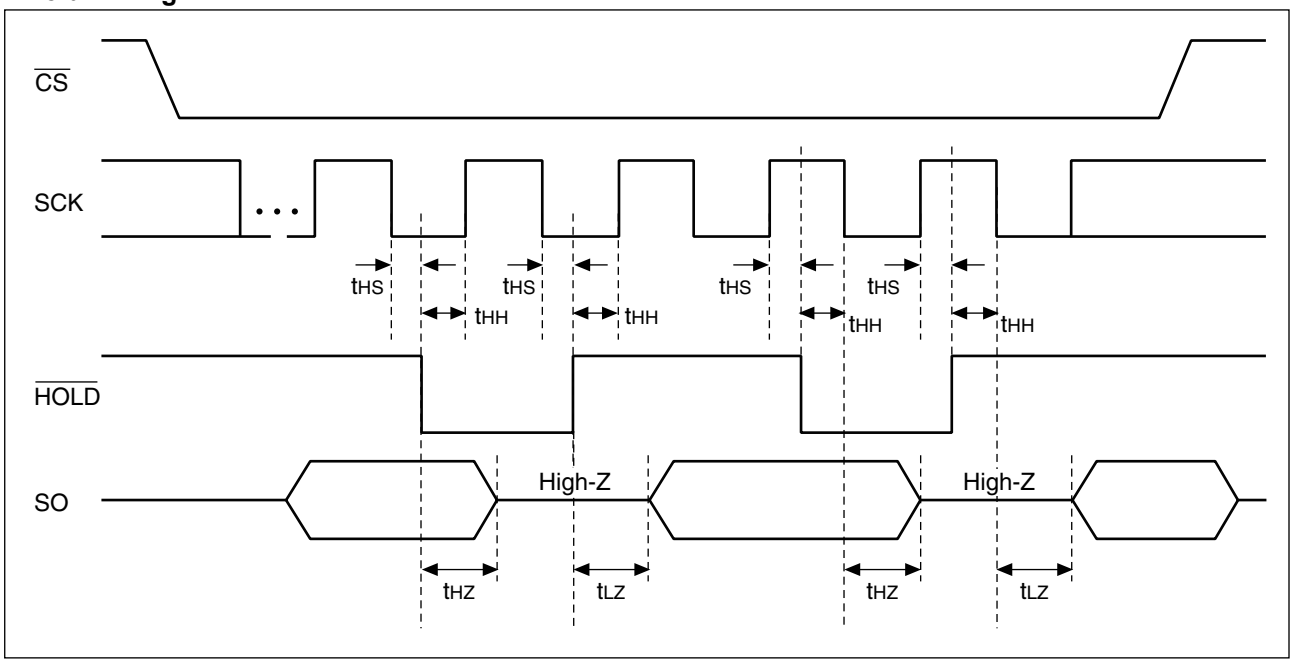
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_O	V_{DD} = 3.3V, V_{IN} = V_{OUT} = 0 V ~ VDD, f = 1 MHz, T_A = +25 °C	—	8	pF
Input capacitance	C_I		—	6	pF

■ TIMING DIAGRAM

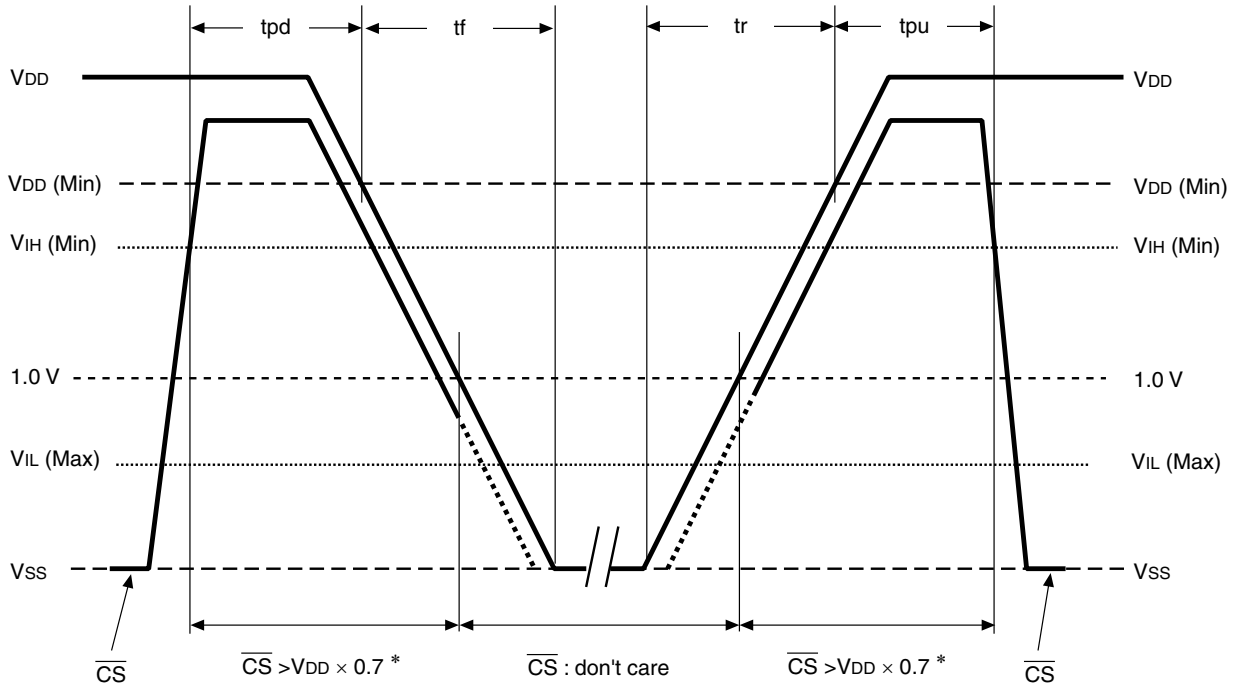
• Serial Data Timing



• Hold Timing



■ POWER ON/OFF SEQUENCE



* : $\overline{CS}$ (Max) < V_{DD} + 0.5 V

Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	400	—	ns
$\overline{CS}$ level hold time at power ON	tpu	250	—	µs
Power supply rising time	tr	0.05	—	ms/V
Power supply falling time	tf	0.1	—	ms/V

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{13}	—	Times/byte	Endurance of the sum of read counts and write counts. Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1 : Total number of reading and writing defines the minimum value of endurance, as an FeRAM memory operates with destructive readout mechanism.

*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

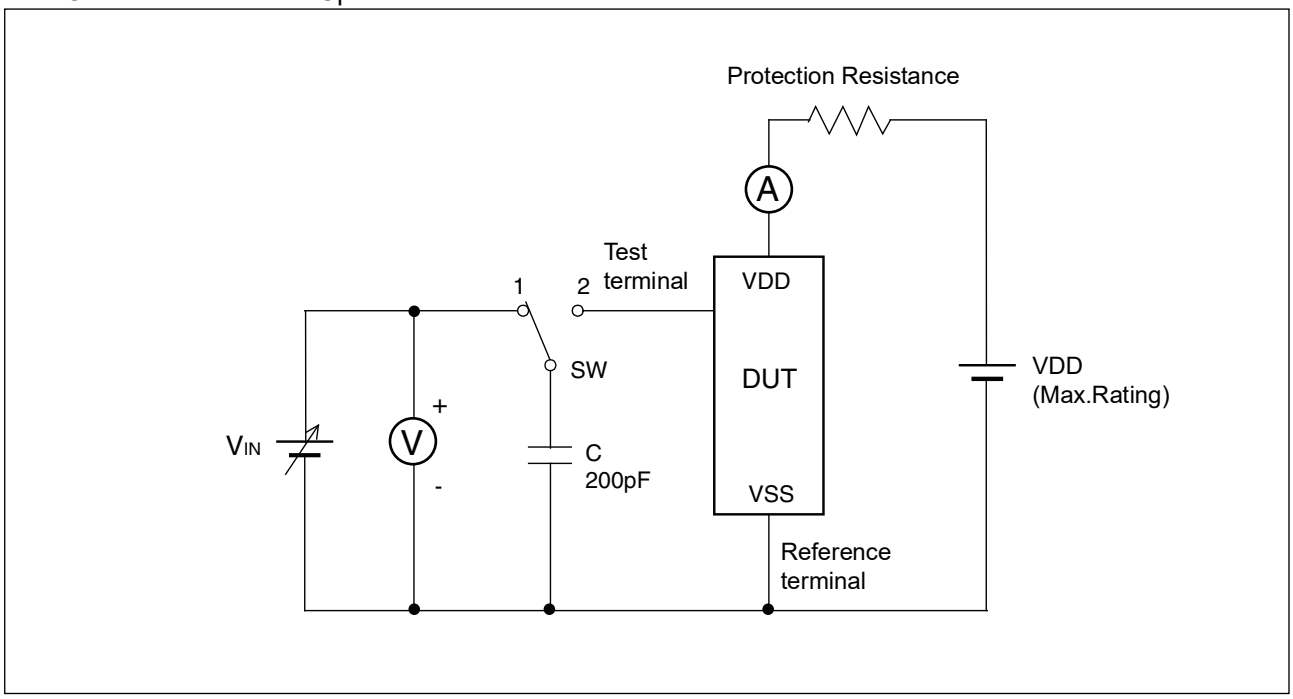
■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS1MTPNF-G-JNE1 MB85RS1MTPNF-G-JNERE1 MB85RS1MTPNF-G-AMERE2 MB85RS1MTPNF-G-AME2 MB85RS1MTPN-G-AMEWE1	≥ |2000 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 1 (IPC/JEDEC J-STD-020E)

MB85RS1MTPNF-G-AME2 /MB85RS1MTPNF-G-AMERE2/ MB85RS1MTPNF-G-AMEWE1

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

MB85RS1MTPNF-G-JNE1 /MB85RS1MTPNF-G-JNERE1

■ Current status on Contained Restricted Substances

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION

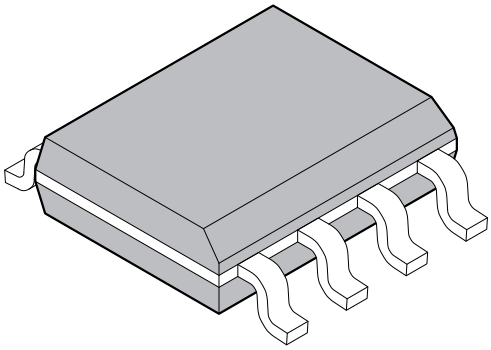
Part number	Package	Shipping form	Minimum shipping quantity
MB85RS1MTPNF-G-JNE1	8-pin plastic SOP	Tube	— *1
MB85RS1MTPNF-G-JNERE1	8-pin plastic SOP	Embossed Carrier tape	1500
MB85RS1MTPNF-G-AMERE2	8-pin plastic SOP	Embossed Carrier tape	1500
MB85RS1MTPNF-G-AME2	8-pin plastic SOP	Tray	— *1
MB85RS1MTPN-G-AMEWE1	8-pin plastic DFN	Embossed Carrier tape	1500

*1 : Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSION

(1)MB85RS1MTPNF-G-JNE1/MB85RS1MTPNF-G-JNERE1
MB85RS1MTPNF-G-AME2/MB85RS1MTPNF-G-AMERE2

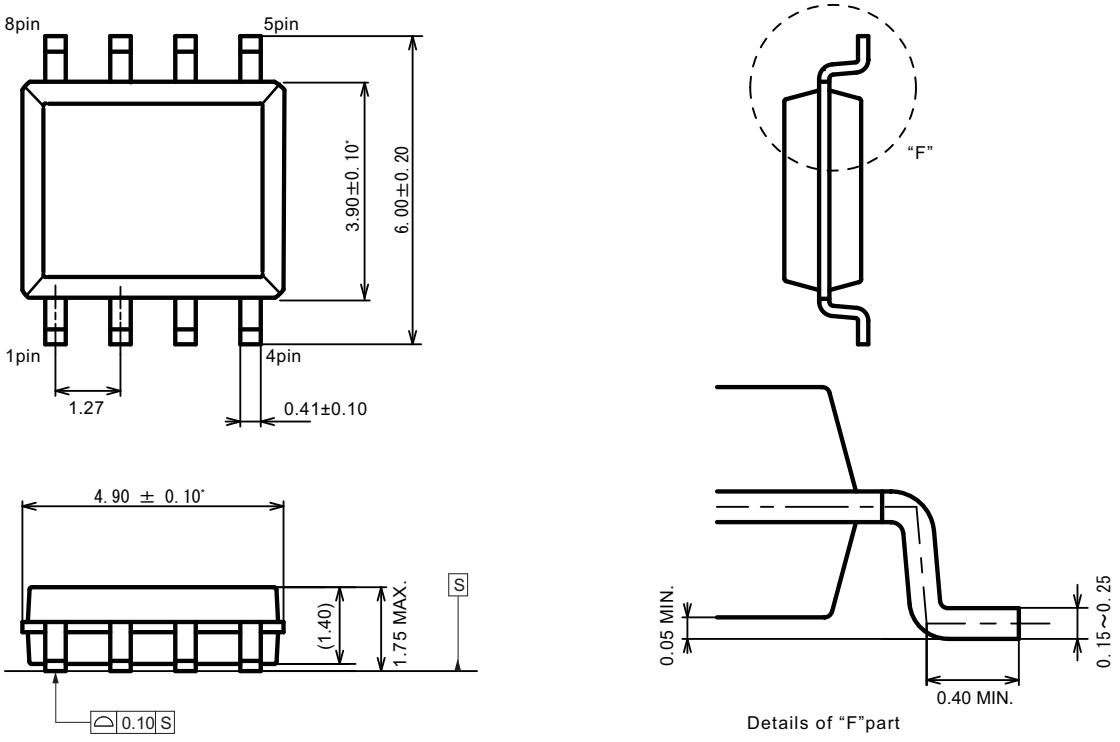
8-pin plastic SOP(150mil)



Lead pitch	1.27mm
Package width x Package length	3.90mm x 4.90mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.75mm MAX.

8-pin plastic SOP

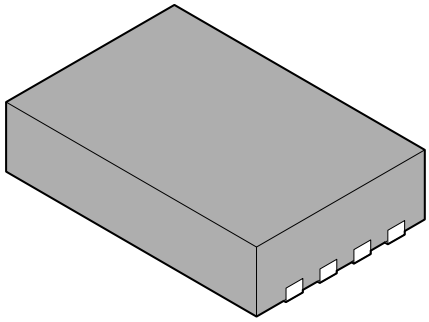
Note *: These dimension do not include resin protrution.
Pins width do not include tie bar cutting remaindar.



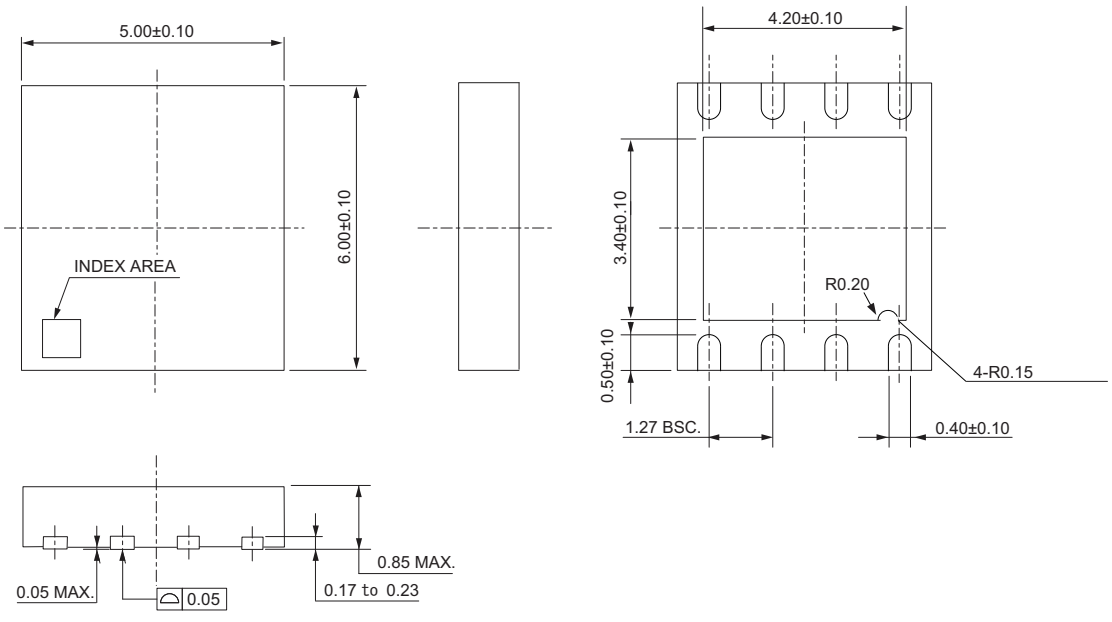
Dimension in mm

(Continued)

(2)MB85RS1MTPN-G-AMEWE1

8-pin plastic DFN 	Lead pitch	1.27 mm
	Package width x Package length	5.00 mm × 6.00 mm
	Sealing method	Plastic mold
	Mounting height	0.85 mm MAX

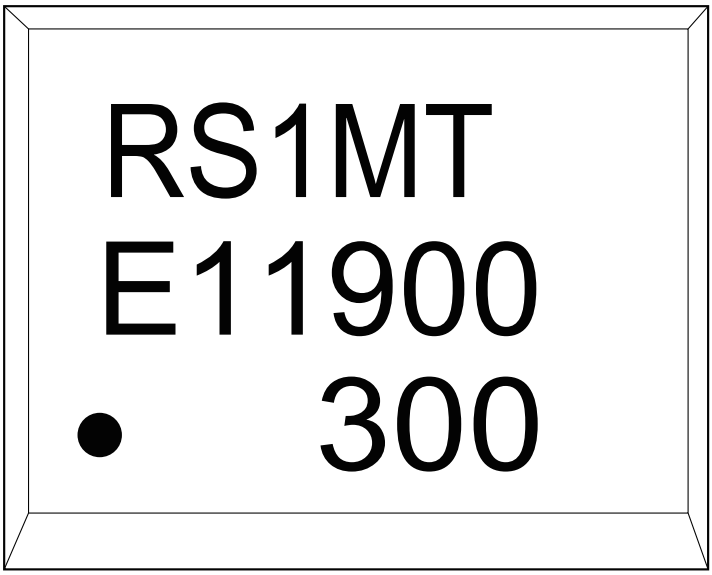
8-pin plastic DFN



Dimensions in mm.

■ MARKING (Example)

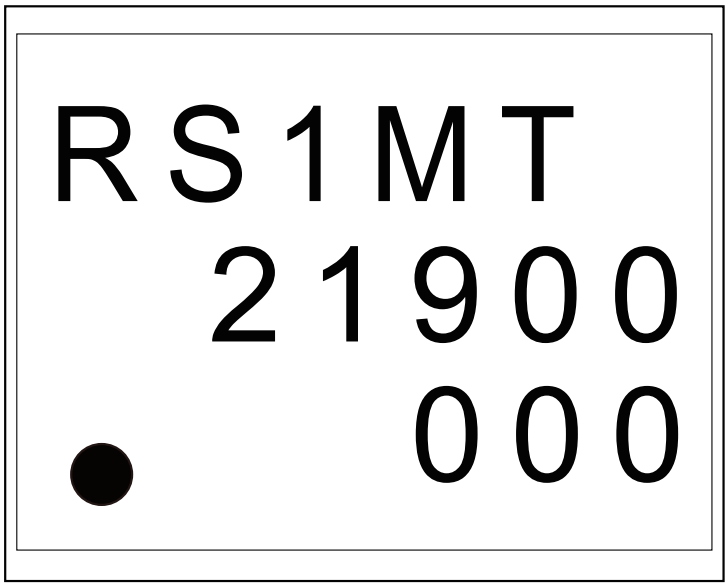
[MB85RS1MTPNF-G-JNE1]
[MB85RS1MTPNF-G-JNERE1]



[8-pin plastic SOP 150mil]

RS1MT: Product name
E11900: E1(Environmental code) + 1900(Year and Week code)
300: Trace code

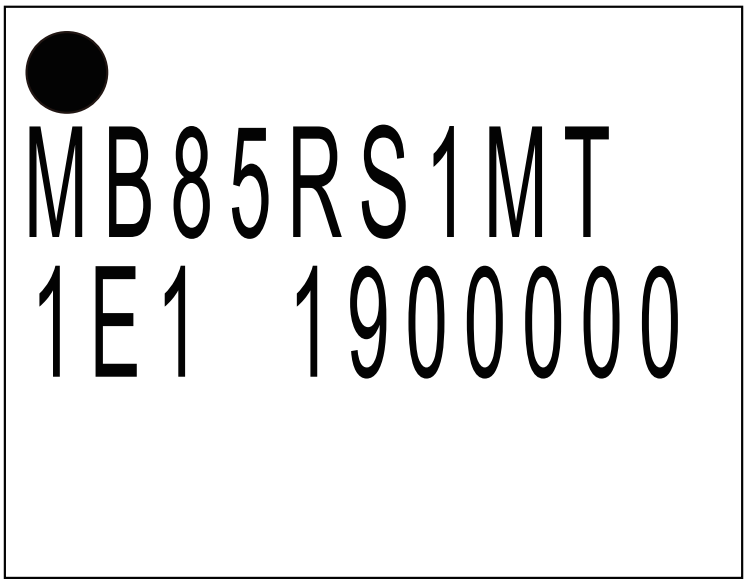
[MB85RS1MTPNF-G-AME2]
[MB85RS1MTPNF-G-AMERE2]



[8-pin plastic SOP 150mil]

RS1MT: Product name
21900: 2(CS code) + 1900(Year and Week code)
000: Trace code

[MB85RS1MTPN-G-AMEWE1]



[8-pin plastic DFN 5mm × 6mm]

MB85RS1MT: Product name
1E1: 1(CS code) + E1(Environmental code)
1900000: 1900(Year and Week code) + 000(Trace code)

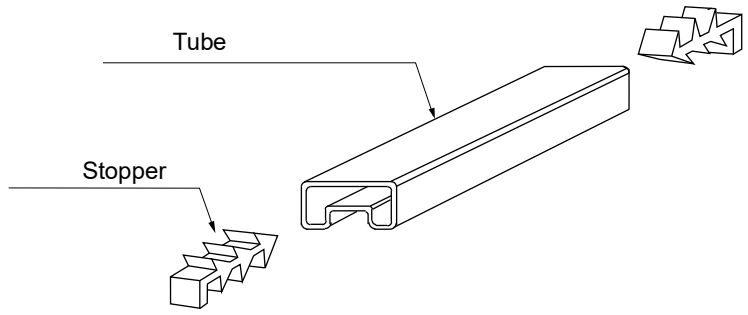
■ PACKING INFORMATION

(1)MB85RS1MTPNF-G-JNE1

1. Tube

1.1 Tube Dimensions

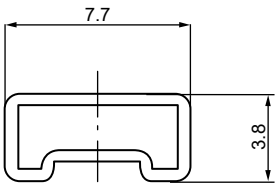
• Tube/stopper shape (example)



• **Tube cross-sections** and Maximum quantity

MB85RS1MTPNF-G-JNE1

Maximum quantity		
ICs/tube	ICs/inner box	ICs/outer box
95	7,600	30,400

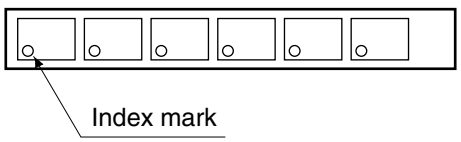


tube length:521

No heat resistance.
Package should not be baked by using tube.

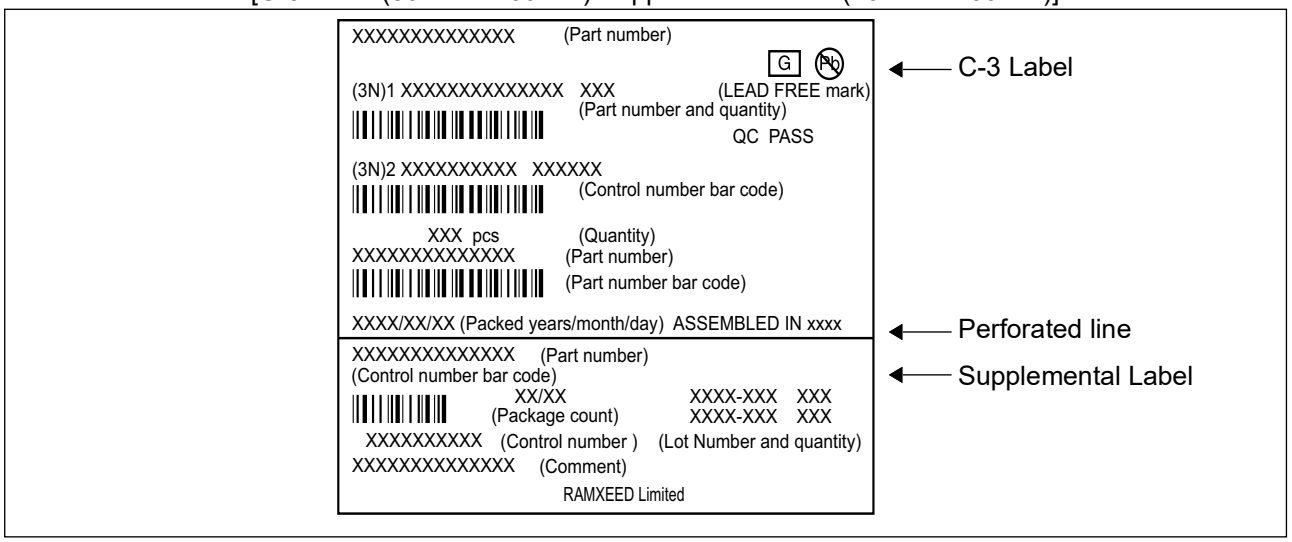
(Dimensions in mm)

• Direction of index in tube



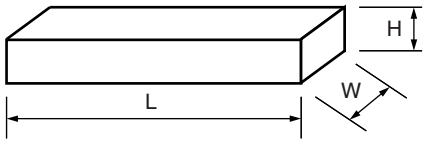
1.2 Product label indicators

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.3 Dimensions for Containers

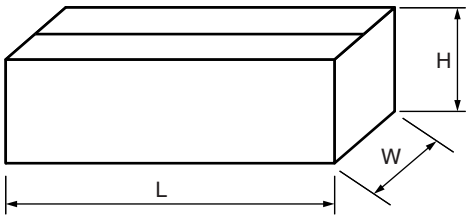
(1) Dimensions for inner box



Part number	L	W	H
MB85RS1MTPNF-G-JNE1	540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



Part number	L	W	H
MB85RS1MTPNF-G-JNE1	565	270	180

(Dimensions in mm)

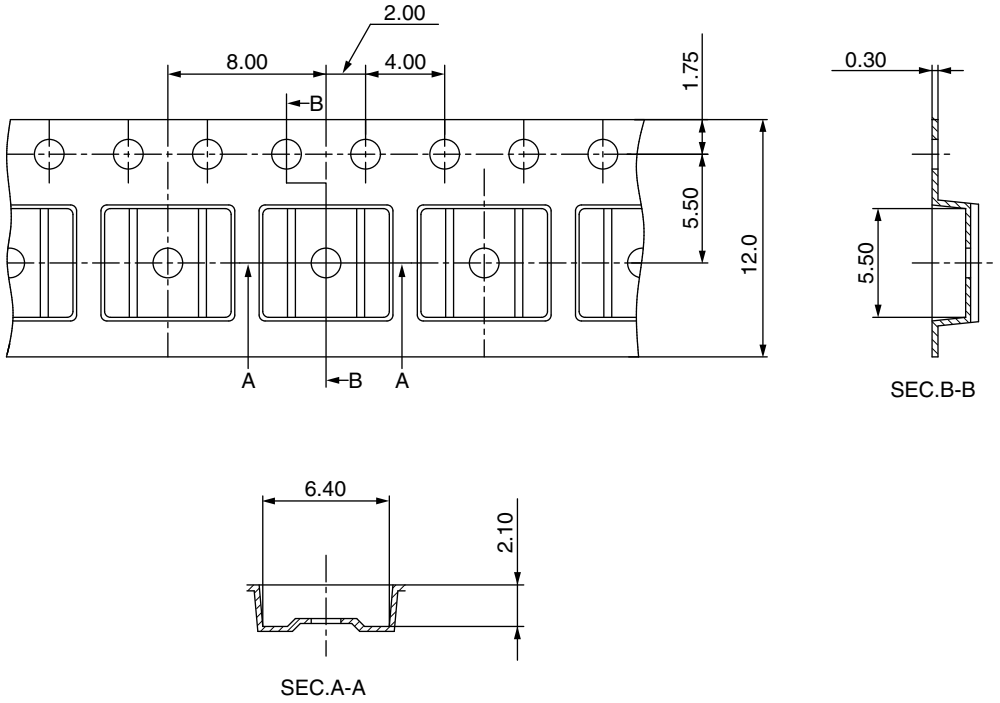
(2)MB85RS1MTPNF-G-JNERE1/MB85RS1MTPNF-G-AMERE2

1. Emboss Tape

1.1 Tape Dimensions (not drawn to scale)(8-pin plastic SOP 150mil)

MB85RS1MTPNF-G-JNERE1/MB85RS1MTPNF-G-AMERE2

Part number	reel diameter (mm)	Maximum storage capacity			MSL Label
		ICs/ reel	ICs/inner box	ICs/outer box	
MB85RS1MTPNF-G-JNERE1	φ330	1,500	1,500 (1 pack/inner box)	10,500 (7 inner boxes/ outer box:Max.)	No
MB85RS1MTPNF-G-AMERE2	φ254	1,500	1,500 (1 pack/inner box)	9,000 (6 inner boxes/ outer box:Max.)	Yes

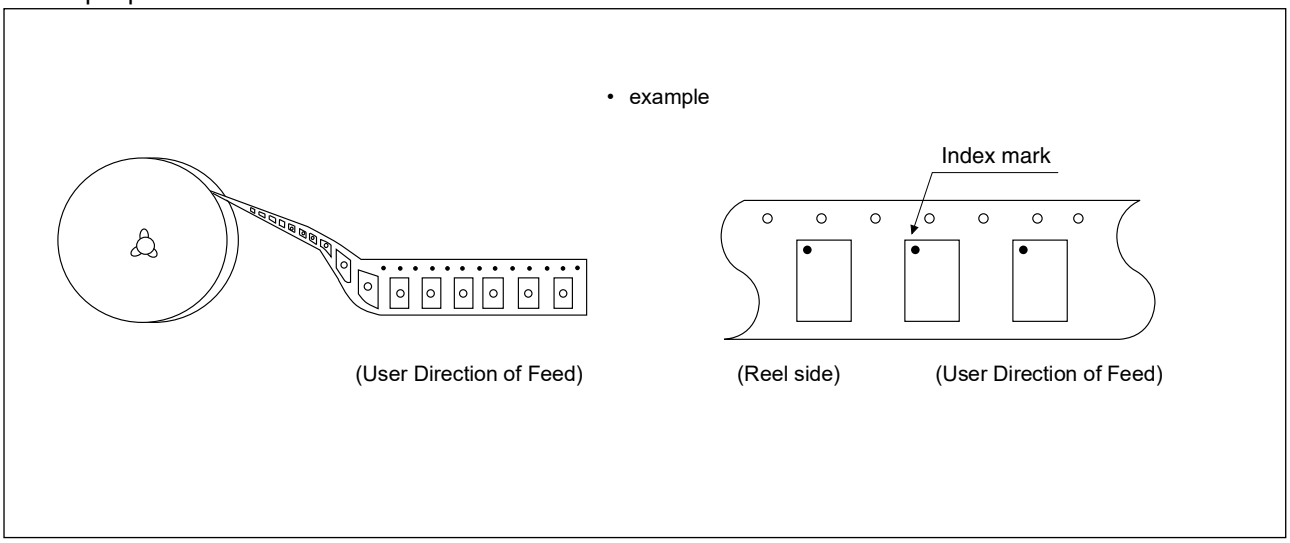


(Dimensions in mm)

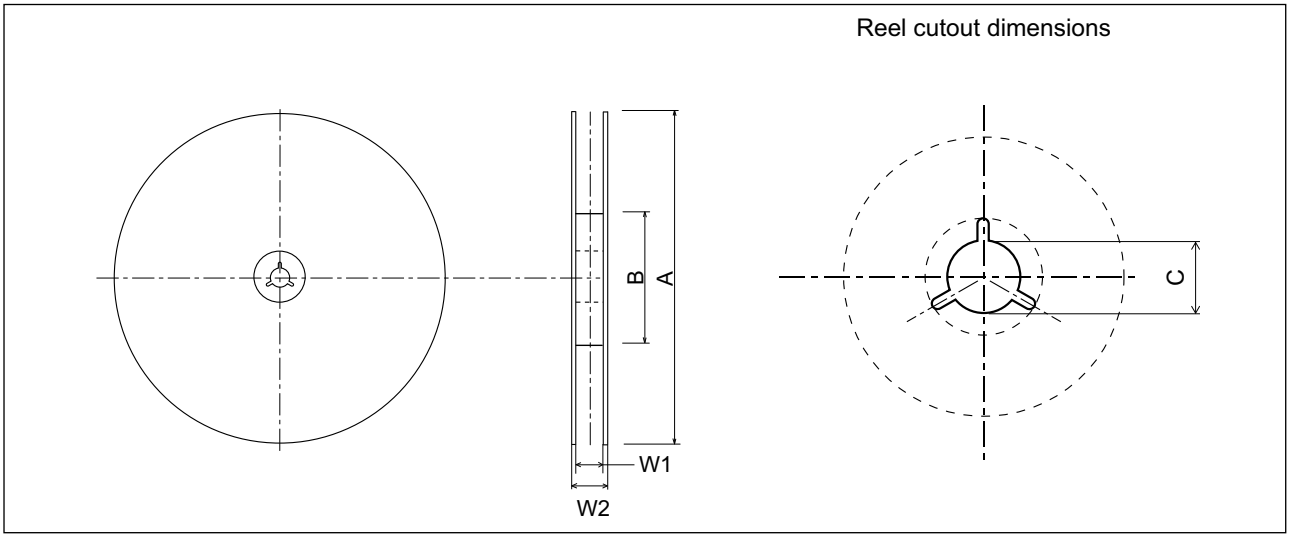
Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

1.2 IC orientation

8-pin plastic SOP 150mil



1.3 Reel dimensions

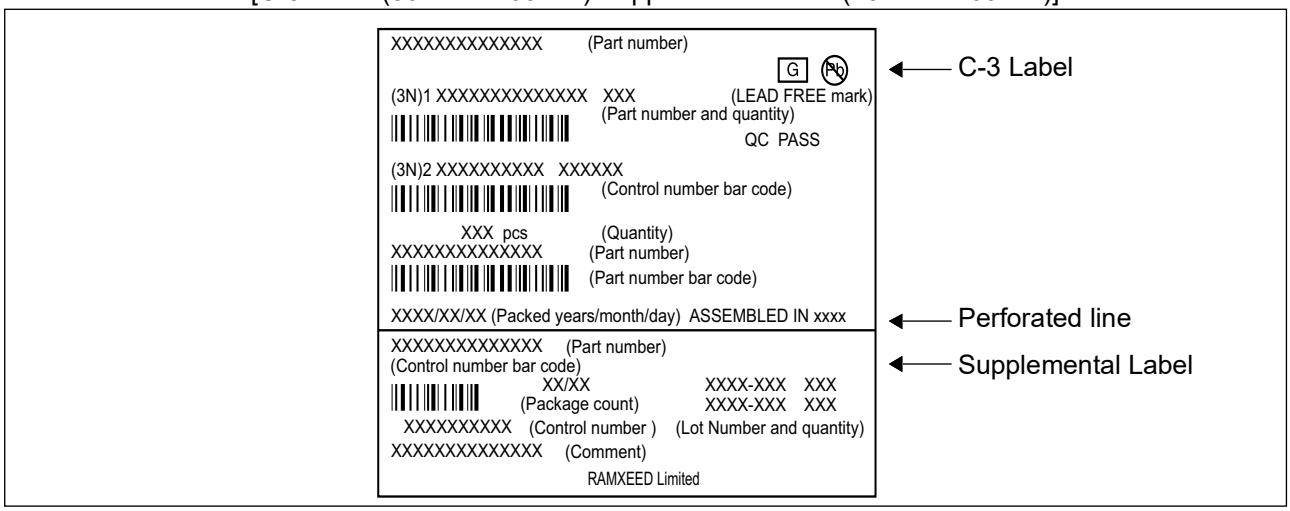


Dimensions in mm

Part number	A	B	C	W1	W2
MB85RS1MTPNF-G-JNERE1	330	100	13	12.4	17.2
MB85RS1MTPNF-G-AMERE2	254	100	13	13.5	17.5

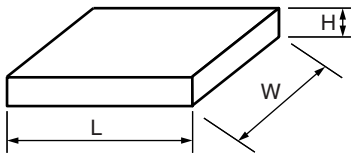
1.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.5 Dimensions for Containers

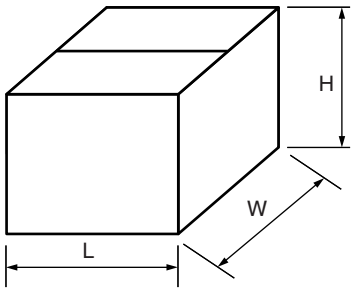
(1) Dimensions for inner box



Part number	L	W	H
MB85RS1MTPNF-G-JNERE1	365	345	40
MB85RS1MTPNF-G-AMERE2	265	260	50

(Dimensions in mm)

(2) Dimensions for outer box



Part number	L	W	H
MB85RS1MTPNF-G-JNERE1	415	400	315
MB85RS1MTPNF-G-AMERE2	565	270	180

(Dimensions in mm)

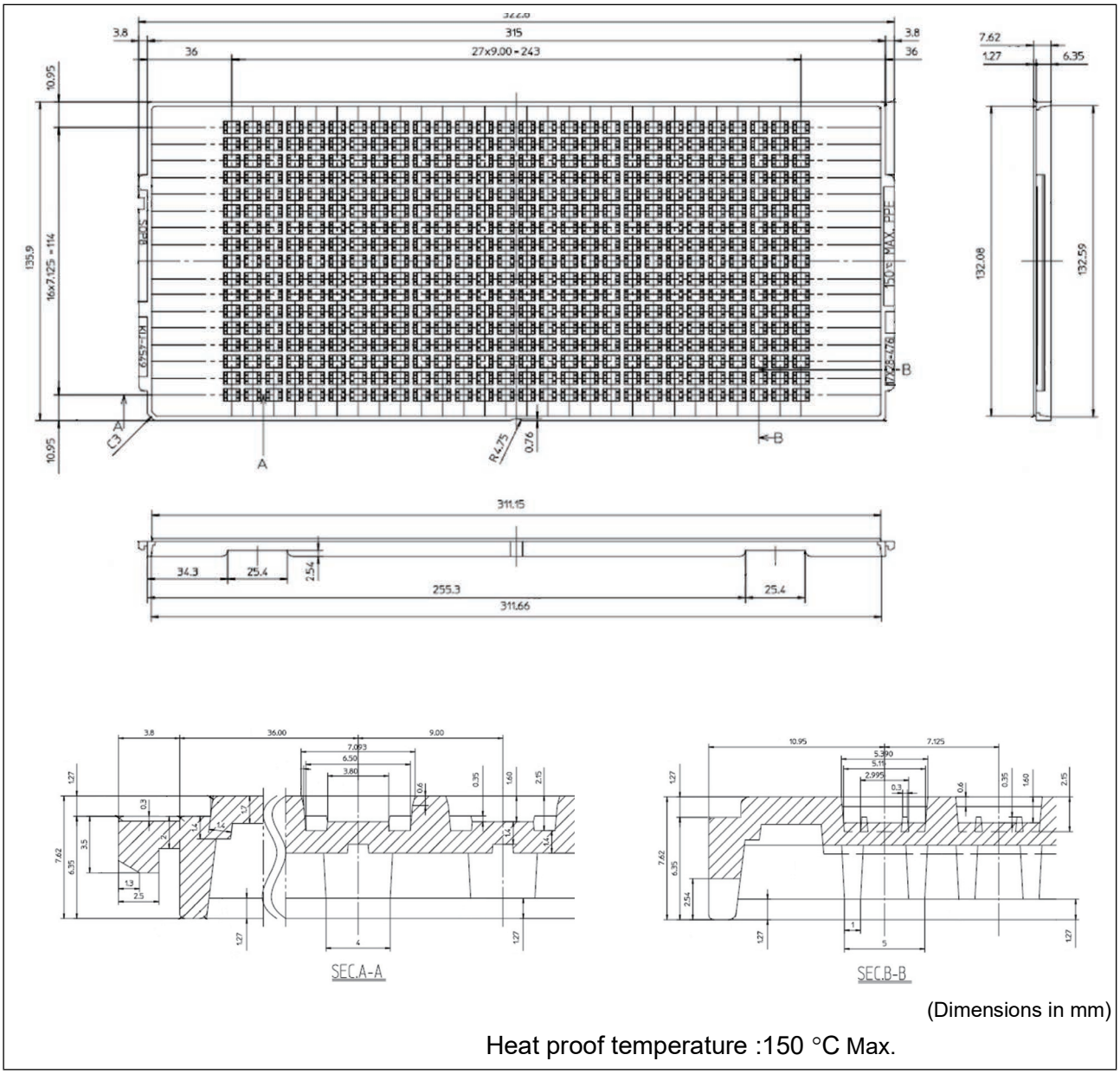
(3)MB85RS1MTPNF-G-AME2

1. Tray

1.1 Tray Storage Capacity

Maximum storage capacity		
ICs/tray	ICs/inner box	ICs/outer box
476	4,760 (Max:10 trays/inner box)	19,040 (Max: 4 inner boxes/outer box)

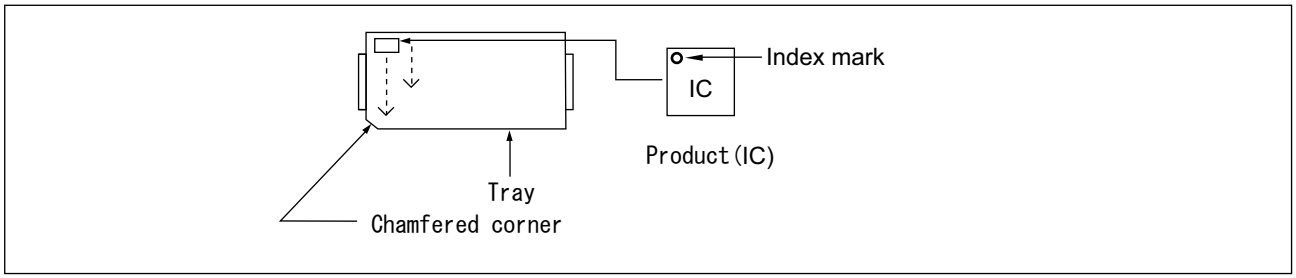
1.2 Tray Dimensions (JEDEC Standard)



(Dimensions in mm)

Heat proof temperature :150 °C Max.

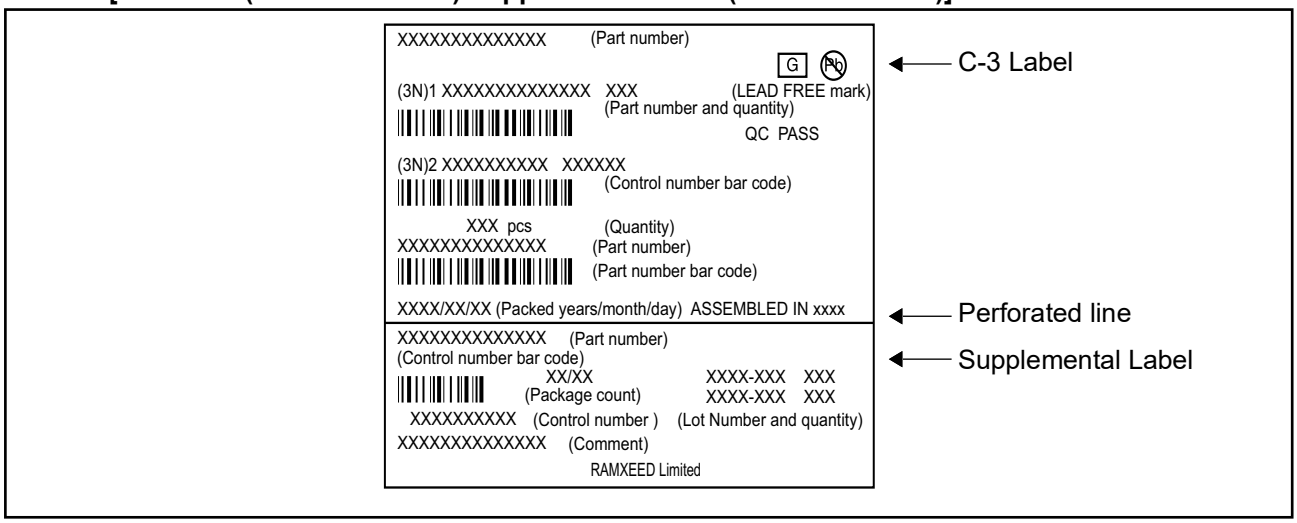
1.3 IC Orientation



1.4 Product label indicators (an example)

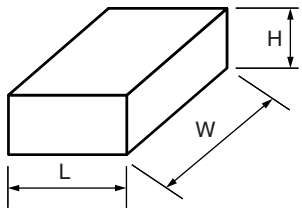
Label on Inner box/Moisture Barrier Bag

[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



1.5 Dimensions for Containers

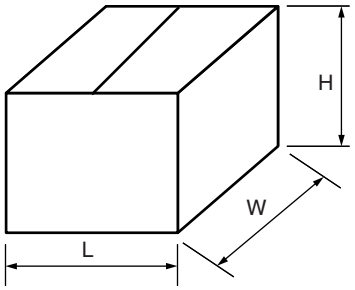
(1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
355	385	195

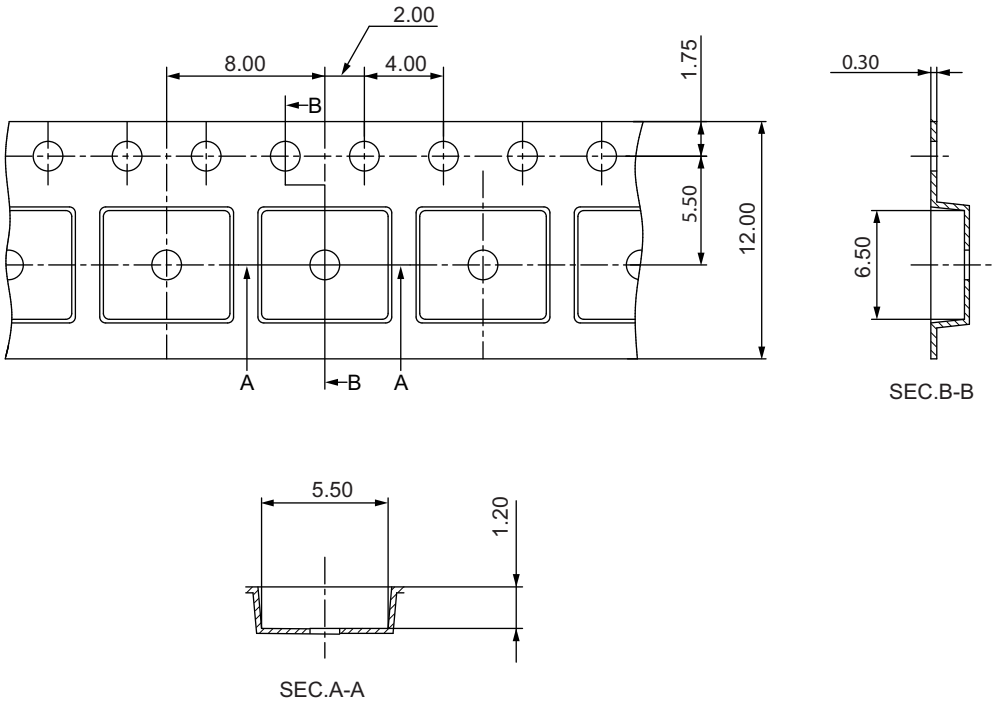
(Dimensions in mm)

(4)MB85RS1MTPN-G-AMEWE1

1. Emboss Tape

1.1 Tape Dimensions (not drawn to scale)(8-pin plastic DFN 5mm × 6mm)

Maximum storage capacity		
ICs/reel(φ254mm)	ICs/inner box	ICs/outer box
1,500	1,500 (1 pack/inner box)	9,000 (6 inner boxes/outer box:Max.)

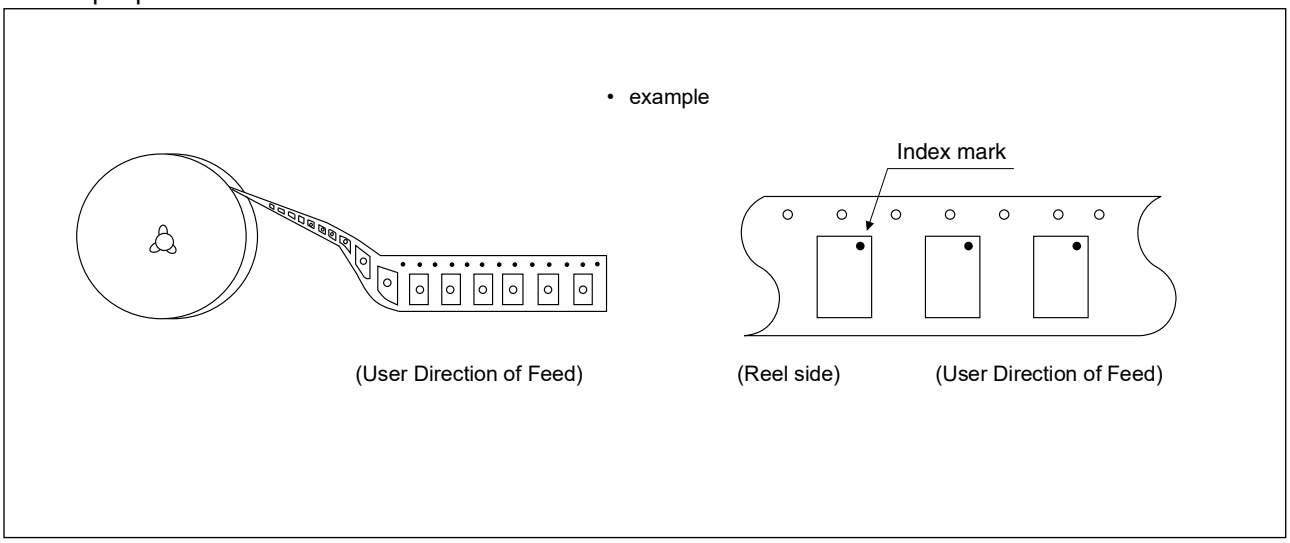


(Dimensions in mm)

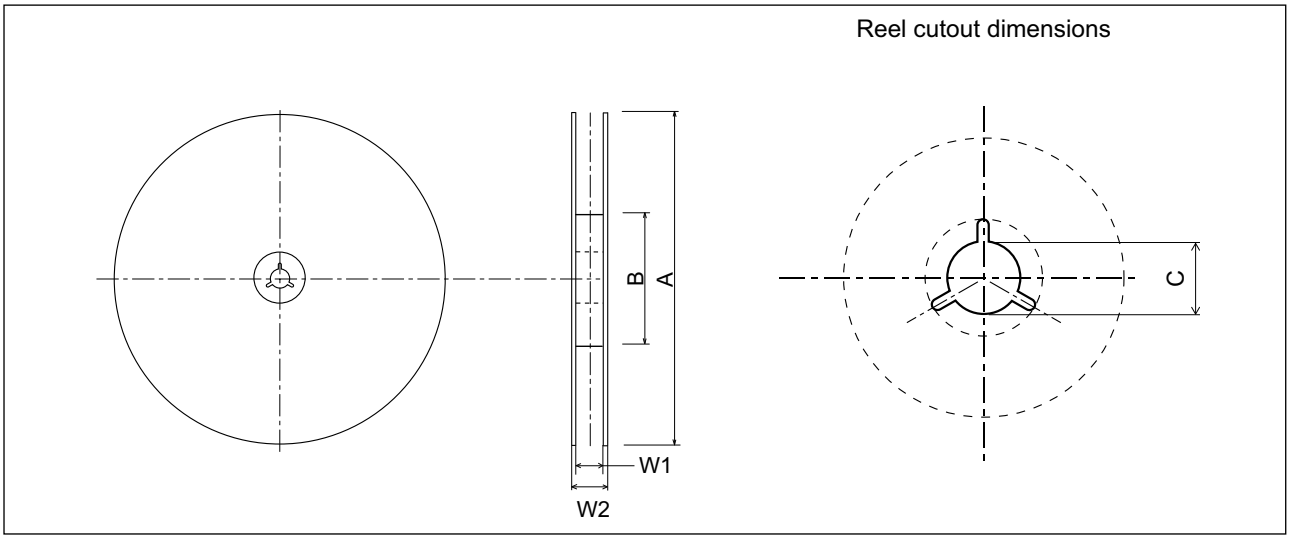
Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

1.2 IC orientation

8-pin plastic DFN 5mm × 6mm



1.3 Reel dimensions

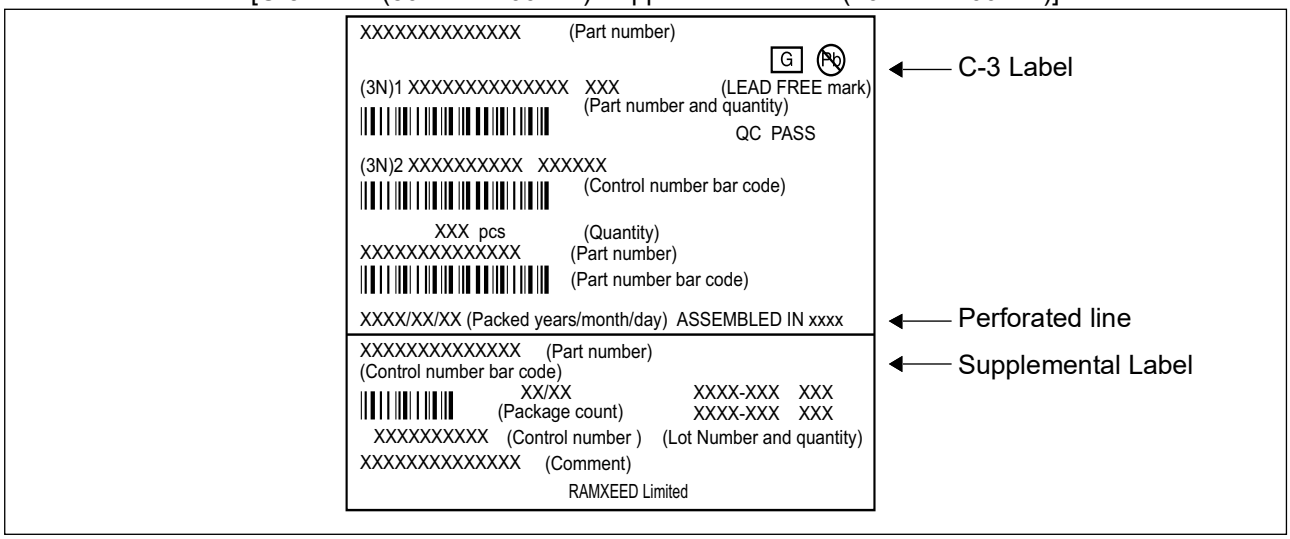


Dimensions in mm

	A	B	C	W1	W2
DFN8	254	100	13	13.5	17.5

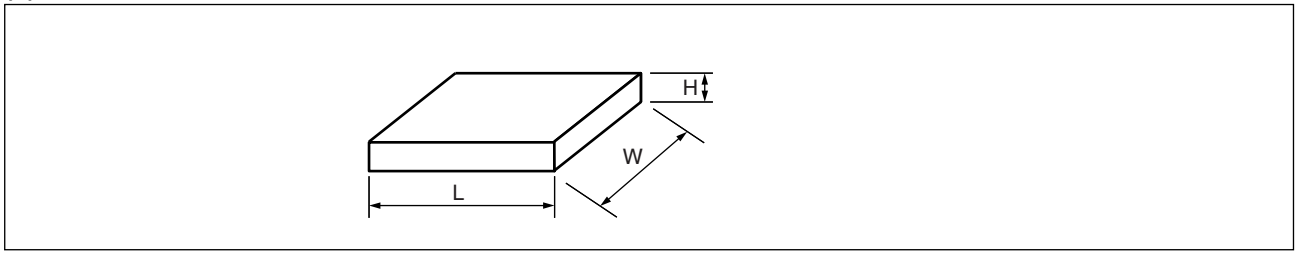
1.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



1.5 Dimensions for Containers

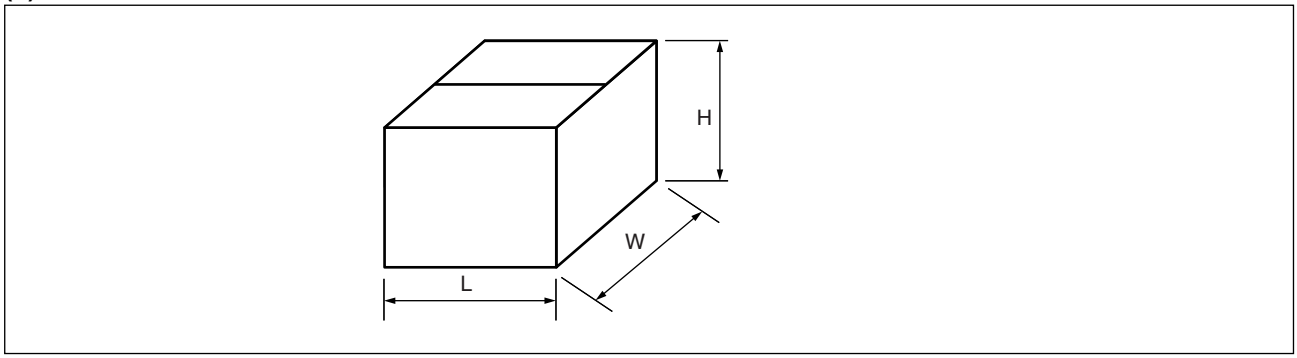
(1) Dimensions for inner box



L	W	H
265	260	50

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
565	270	180

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
2	PIN ASSIGNMENT	Change DFN8 Pin Assignment.
19	REFLOW CONDITIONS AND FLOOR LIFE	Add MSL1 information.
20	ORDERING INFORMATION	Change Part number for SOP8 and DFN8.
22	PACKAGE DIMENSION	Change DFN8 package dimension for new parts number.
24	MARKING (Example)	Change Marking information for new parts number.
25~	PACKING INFORMATION	Packaging information change due to part number change.

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