Memory FeRAM

2 M (256 K × 8) Bit SPI

MB85RS2MTA

■ DESCRIPTION

MB85RS2MTA is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 262,144 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85RS2MTA adopts the Serial Peripheral Interface (SPI).
The MB85RS2MTA is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85RS2MTA can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
MB85RS2MTA does not take long time to write data like Flash memories or E^2PROM, and MB85RS2MTA takes no wait time.

■ FEATURES

- Bit configuration : 262,144 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 40MHz (Max)

- High endurance : 10^{14} times
- Data retention : 10 years (+85 °C), 95 years(+55 °C)
- Operating power supply voltage : 1.7 V to 3.6 V
- Low power consumption : Operating power supply current 2.3mA (Max@40 MHz)
  Standby current 50 μA (Max)
  Sleep current 10 μA (Max)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 8-pin plastic SOP
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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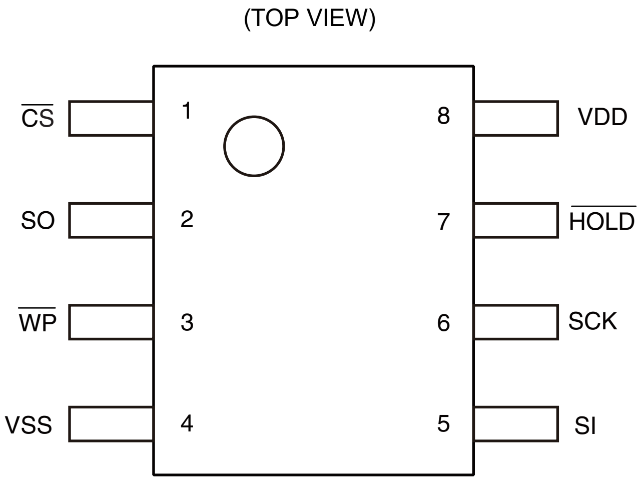
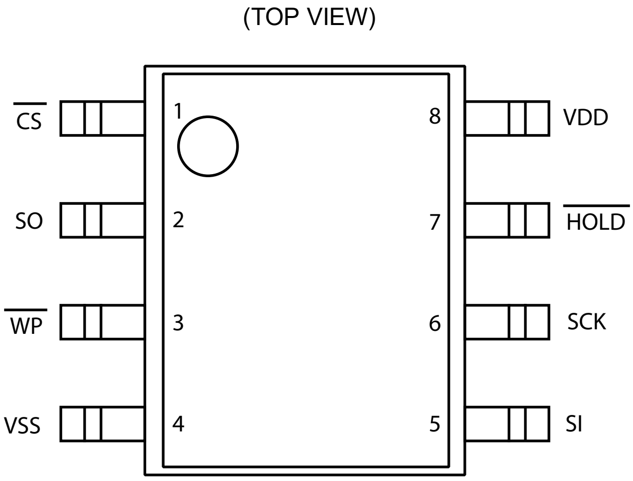
■ PIN ASSIGNMENT



(8-pin plastic SOP, 150mil)

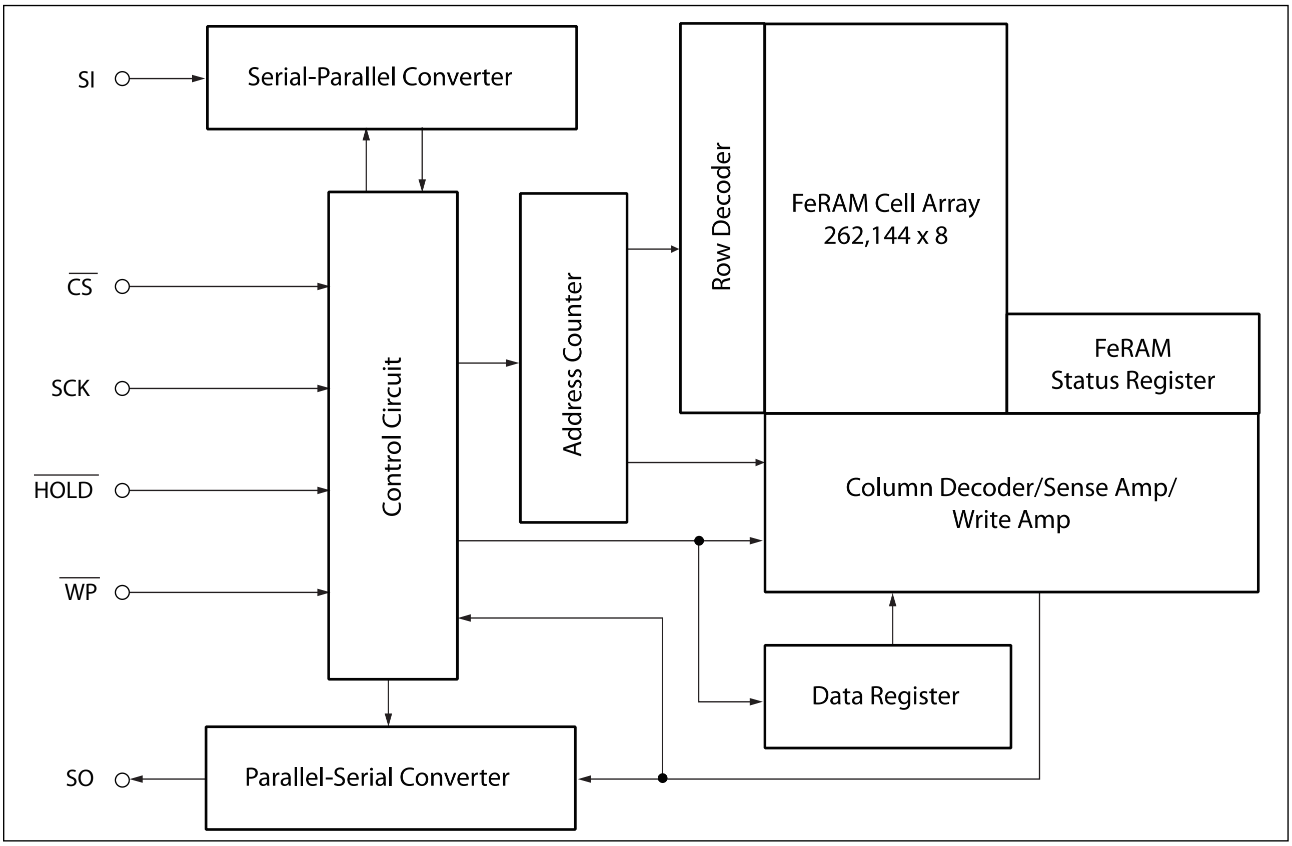


(8-pin plastic SOP, 208mil)

■ PIN FUNCTIONAL DESCRIPTIONS

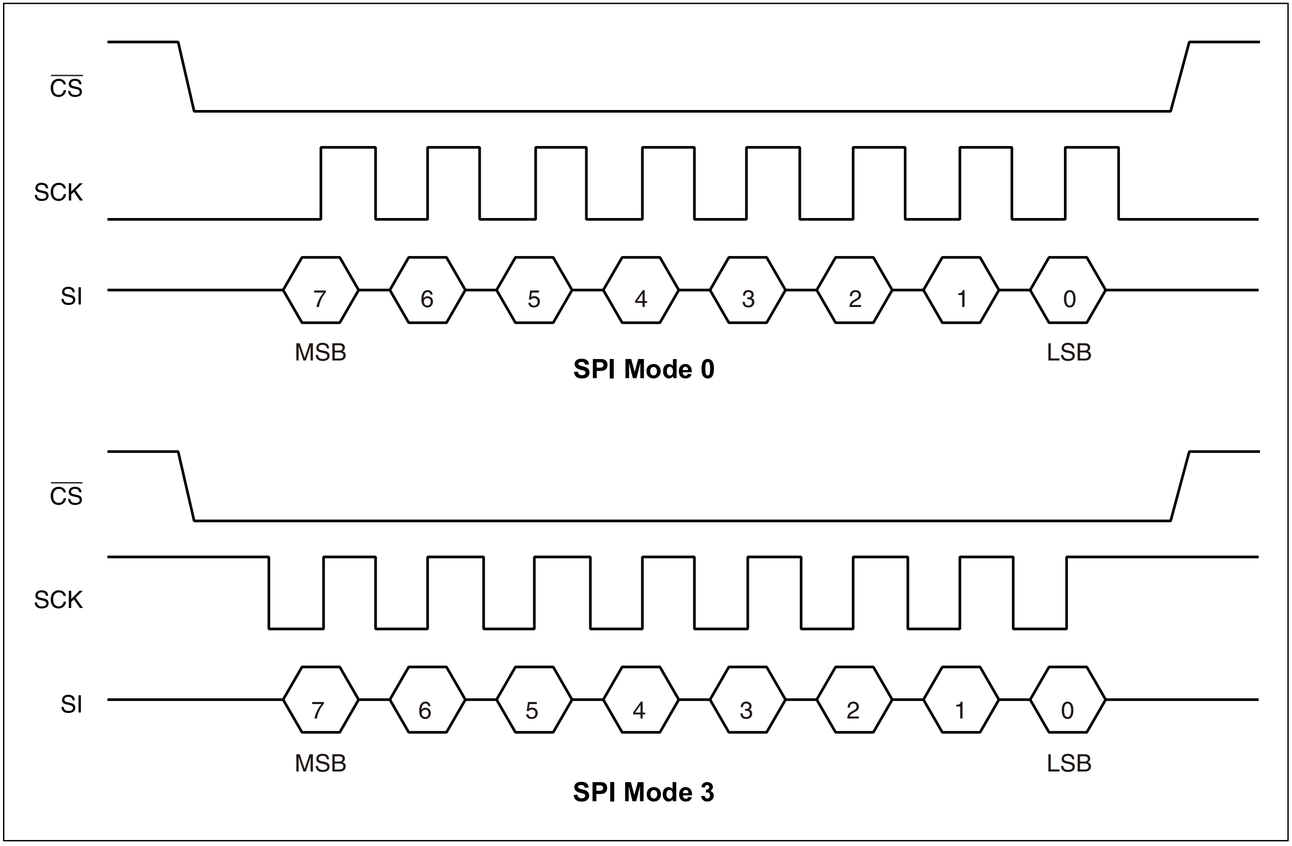
Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is “L” level, device is in select (active) status. $\overline{CS}$ has to be “L” level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in related with $\overline{WP}$ and WPEN. See “■WRITING PROTECT” for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is “L” level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See “■HOLD OPERATION” for detail.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

■ BLOCK DIAGRAM


SI
CS
SCK
HOLD
WP
SO
Serial-Parallel Converter
Control Circuit
Address Counter
Row Decoder
FeRAM Cell Array
262,144 x 8
FeRAM
Status Register
Column Decoder/Sense Amp/
Write Amp
Data Register
Parallel-Serial Converter

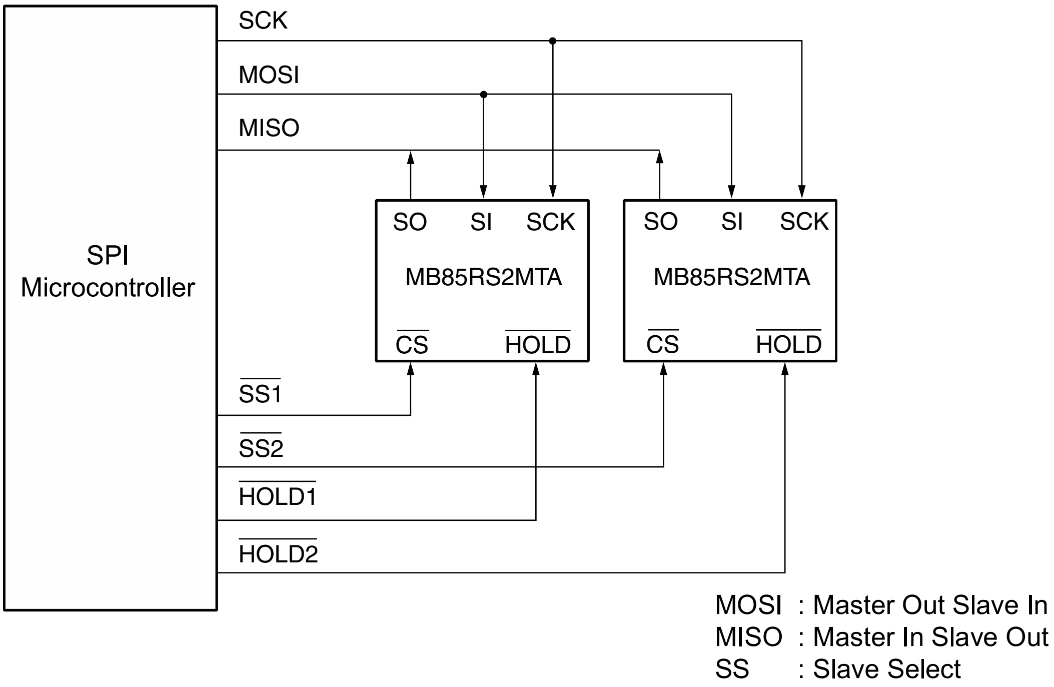
■ SPI MODE

MB85RS2MTA corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .

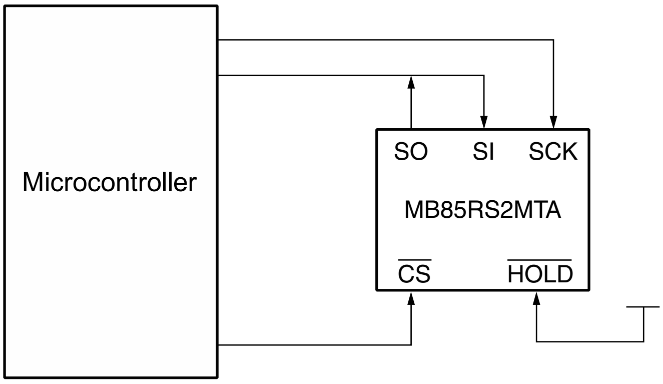

CS
SCK
SI
7
6
5
4
3
2
1
0
MSB
LSB
SPI Mode 0
CS
SCK
SI
7
6
5
4
3
2
1
0
MSB
LSB
SPI Mode 3

■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS2MTA works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.


SPI
Microcontroller
SCK
MOSI
MISO
SS1
SS2
HOLD1
HOLD2
SO
SI
SCK
MB85RS2MTA
CS
HOLD
SO
SI
SCK
MB85RS2MTA
CS
HOLD
MOSI : Master Out Slave In
MISO : Master In Slave Out
SS : Slave Select

System Configuration with SPI Port


Microcontroller
SO
SI
SCK
MB85RS2MTA
CS
HOLD

System Configuration without SPI Port

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to “■WRITING PROTECT”) relating with $\overline{\text{WP}}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to “■BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. After power ON. After WRDI command recognition. After return from “SLEEP mode” mode. This device supports continual programming mode. After the following operations, without reseting WEL, this device can be programmed continually. After WRSR command. After WRITE command.
0	0	This is a bit fixed to “0”.

■ OP-CODE

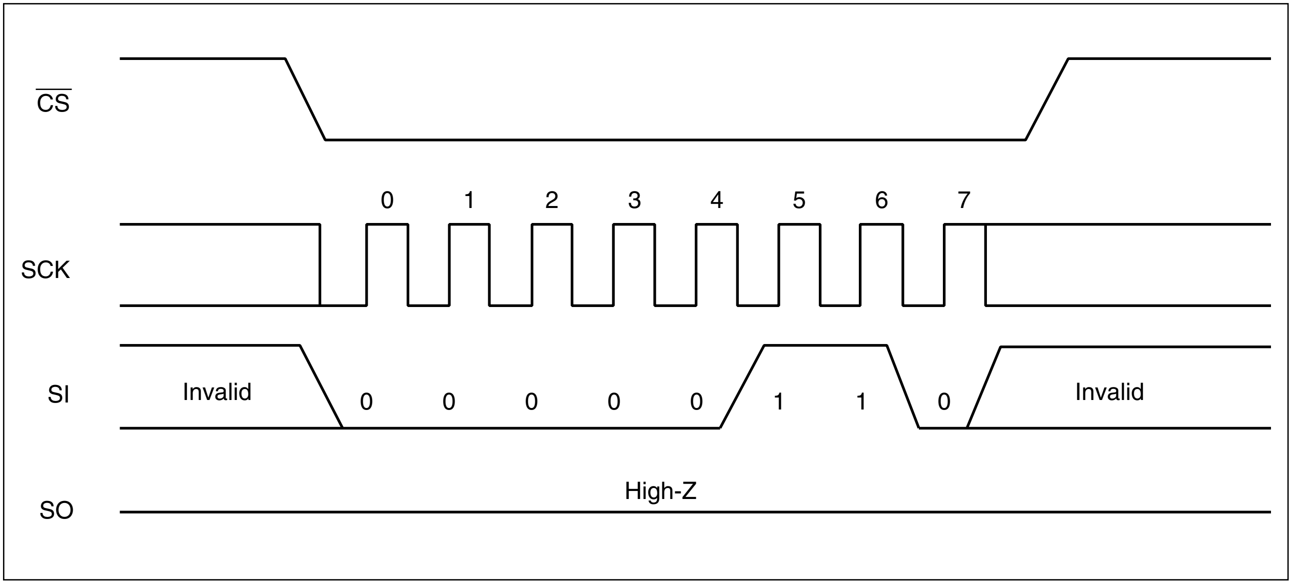
MB85RS2MTA accepts 9 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{\text{CS}}$ is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110$_B$
WRDI	Reset Write Enable Latch	0000 0100$_B$
RDSR	Read Status Register	0000 0101$_B$
WRSR	Write Status Register	0000 0001$_B$
READ	Read Memory Code	0000 0011$_B$
WRITE	Write Memory Code	0000 0010$_B$
RDID	Read Device ID	1001 1111$_B$
FSTRD	Fast Read Memory Code	0000 1011$_B$
SLEEP	Sleep Mode	1011 1001$_B$

■ COMMAND

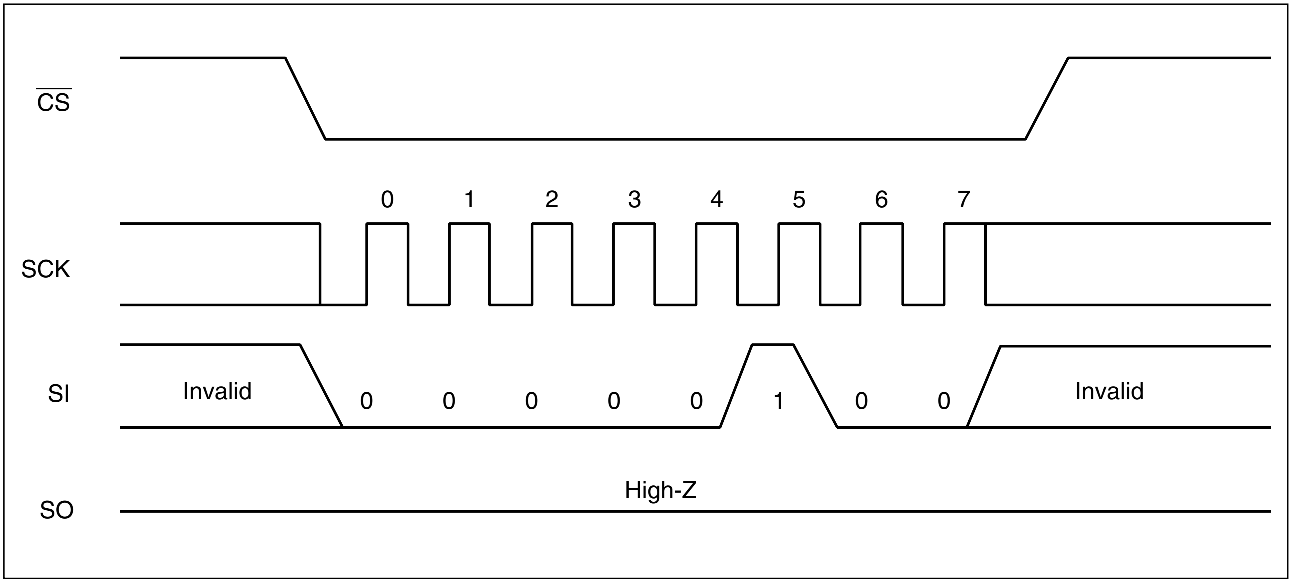
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .


CS
SCK
SI
SO
0
1
2
3
4
5
6
7
Invalid
0
0
0
0
0
1
1
0
Invalid
High-Z

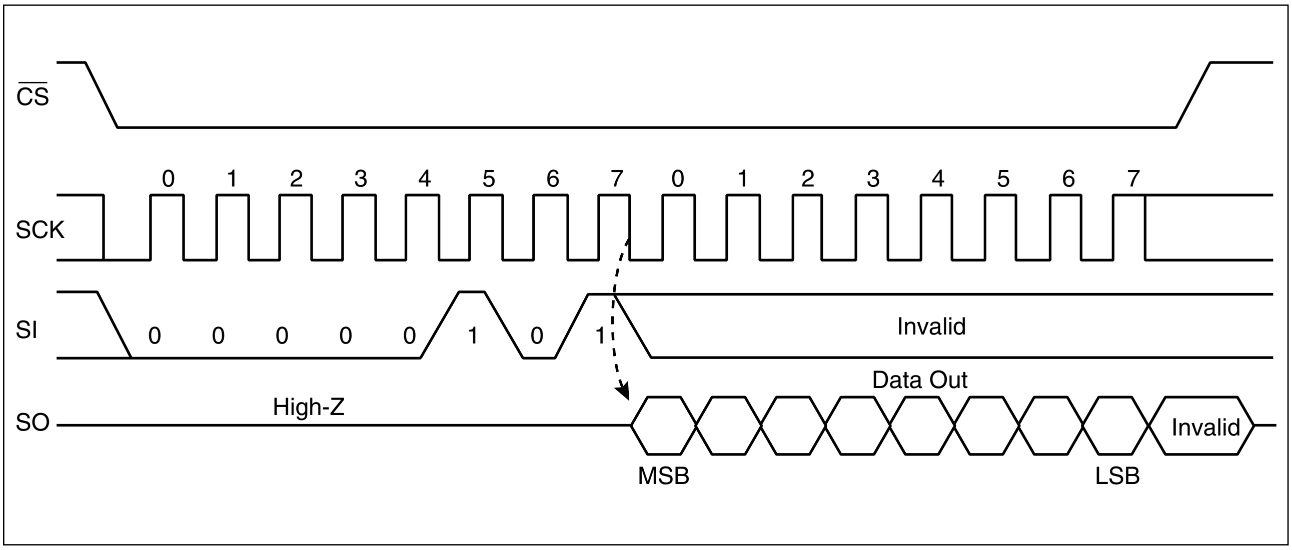
• WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.


CS
SCK
SI
SO
0
1
2
3
4
5
6
7
Invalid
0
0
0
0
0
1
0
0
Invalid
High-Z

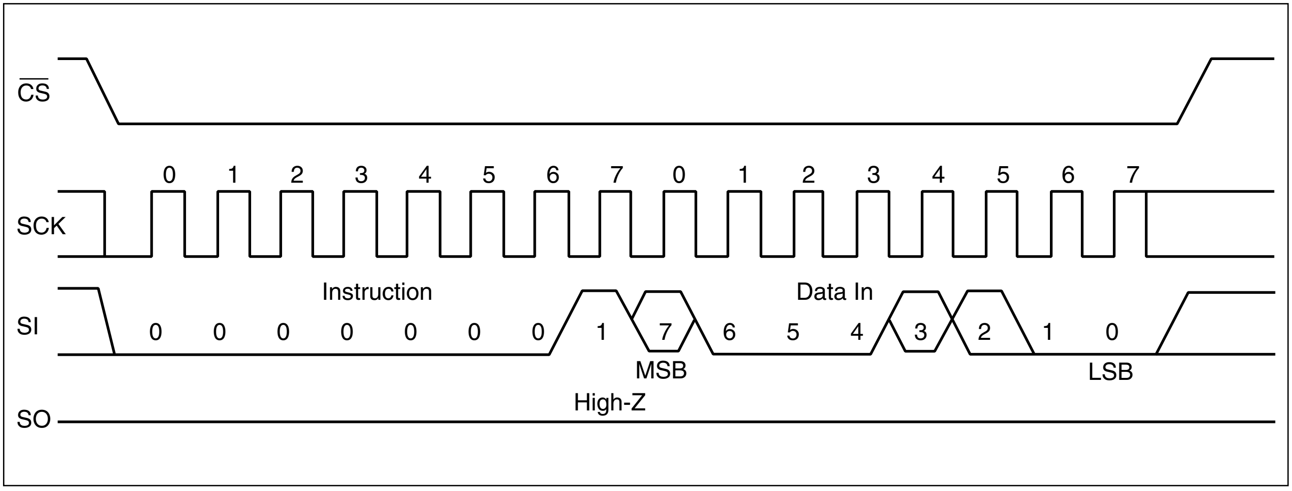
- **RDSR**

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
0 0 0 0 0 1 0 1
Invalid
High-Z
Data Out
Invalid
MSB
LSB

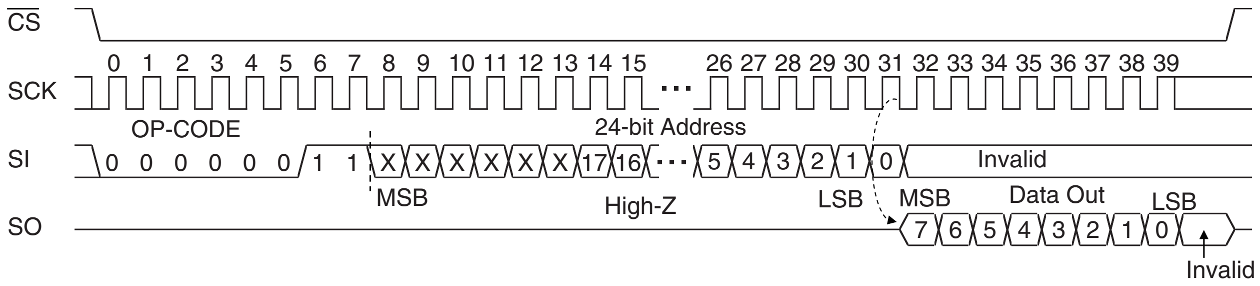
- **WRSR**

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{WP}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence.


CS
SCK
SI
SO
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
Instruction
0 0 0 0 0 0 0 1
Data In
7 6 5 4 3 2 1 0
MSB
LSB
High-Z

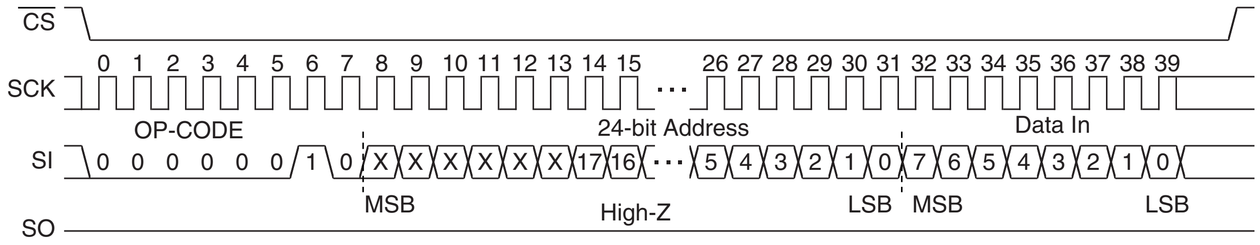
- **READ**

The READ command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{\text{CS}}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{\text{CS}}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.


CS
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 26 27 28 29 30 31 32 33 34 35 36 37 38 39
SCK
OP-CODE
24-bit Address
SI
0 0 0 0 0 0 1 1 X X X X X X 17 16 ··· 5 4 3 2 1 0
Invalid
MSB
High-Z
LSB
MSB
Data Out
LSB
SO
7 6 5 4 3 2 1 0
Invalid

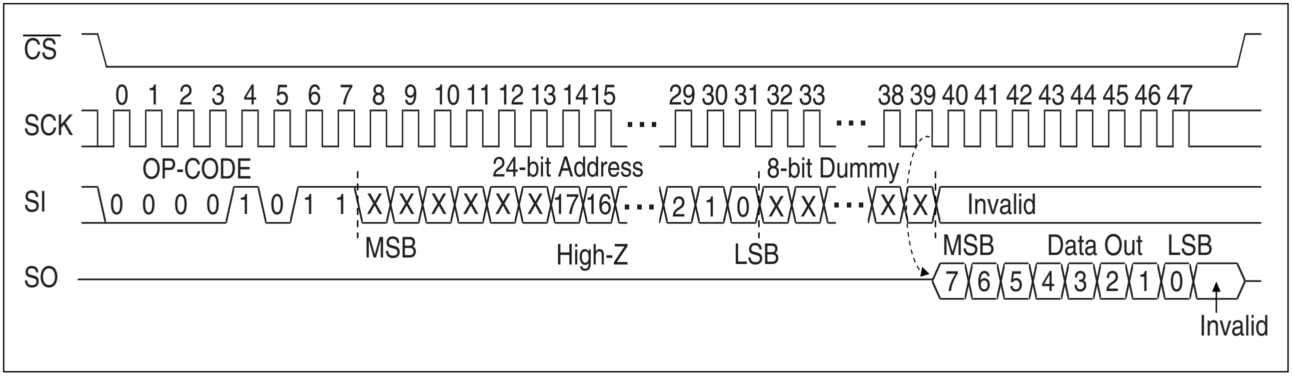
- **WRITE**

The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 6-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen $\overline{\text{CS}}$ will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before $\overline{\text{CS}}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.


CS
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 26 27 28 29 30 31 32 33 34 35 36 37 38 39
SCK
OP-CODE
24-bit Address
Data In
SI
0 0 0 0 0 0 1 0 X X X X X X 17 16 ··· 5 4 3 2 1 0 7 6 5 4 3 2 1 0
MSB
High-Z
LSB
MSB
LSB
SO

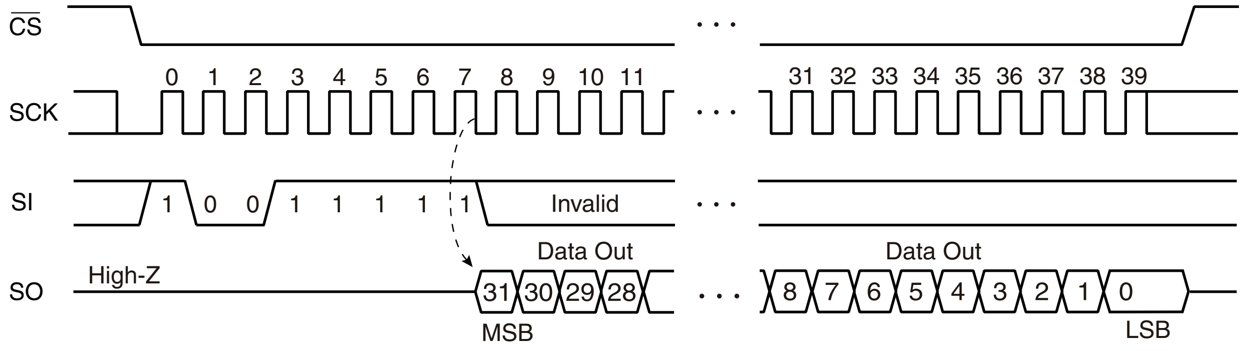
- **FSTRD**

The FSTRD command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 6-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
29 30 31 32 33
38 39 40 41 42 43 44 45 46 47
OP-CODE
24-bit Address
8-bit Dummy
SI
0 0 0 0 1 0 1 1
X X X X X X 17 16
2 1 0 X X
X X
Invalid
MSB
High-Z
LSB
MSB
Data Out
LSB
SO
7 6 5 4 3 2 1 0
Invalid

- **RDID**

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen.


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11
31 32 33 34 35 36 37 38 39
SI
1 0 0 1 1 1 1 1
Invalid
SO
High-Z
Data Out
31 30 29 28
MSB
Data Out
8 7 6 5 4 3 2 1 0
LSB

	bit									
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Hex**	
Manufacturer ID	0	0	0	0	0	1	0	0	04_{H}	RAMXEED
Continuation code	0	1	1	1	1	1	1	1	$7F_{H}$	

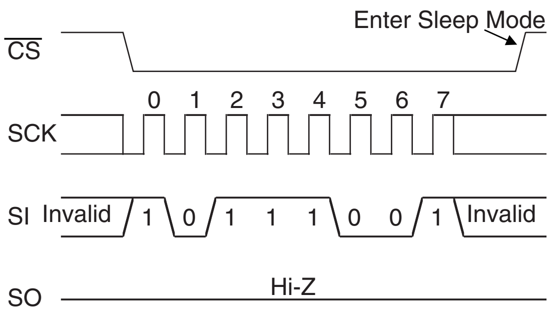
	Proprietary use			**Density**					**Hex**	
Product ID (1st Byte)	0	1	0	0	1	0	0	0	48_{H}	Density: 01000_{B} = 2 Mbit

	Proprietary use								**Hex**	
Product ID (2nd Byte)	0	0	0	0	0	0	1	1	03_{H}	

- **SLEEP**

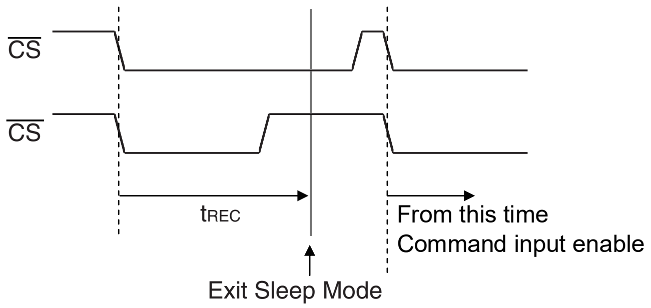
The SLEEP command shifts the LSI to a low power mode called “SLEEP mode”. The transition to the SLEEP mode is carried out at the rising edge of $\overline{\text{CS}}$ after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of $\overline{\text{CS}}$ after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are logically ignored and SO changes to a Hi-Z state. In case all other pins are not fixed to VDD or VSS than $\overline{\text{CS}}$, a through-current may flow.


Enter Sleep Mode
CS
0 1 2 3 4 5 6 7
SCK
SI
Invalid
1 0 1 1 1 0 0 1
Invalid
SO
Hi-Z

Sleep Mode Entry

Returning to an normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 µs) time from the falling edge of $\overline{\text{CS}}$ (see the figure below). It is possible to return $\overline{\text{CS}}$ to H level before t_{REC} time. However, it is prohibited to bring down $\overline{\text{CS}}$ to L level again during t_{REC} period.


CS
CS
tREC
From this time
Command input enable
Exit Sleep Mode

Sleep Mode Exit

■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

BP1	BP0	Protected Block
0	0	None
0	1	30000_H to $3FFFF_H$ (upper 1/4)
1	0	20000_H to $3FFFF_H$ (upper 1/2)
1	1	00000_H to $3FFFF_H$ (all)

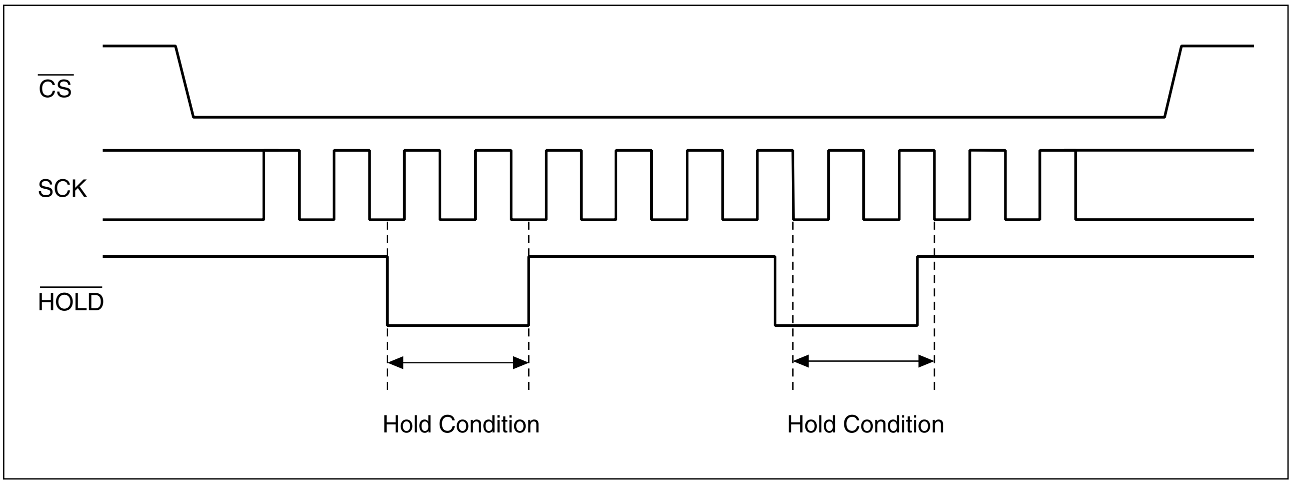
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{\text{WP}}$ as shown in the table.

WEL	WPEN	$\overline{\text{WP}}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{\text{HOLD}}$ is "L" level while $\overline{\text{CS}}$ is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a $\overline{\text{HOLD}}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{\text{HOLD}}$ pin transited to "L" level when SCK is "L" level, return the $\overline{\text{HOLD}}$ pin to "H" level at SCK being "L" level. In the same manner, in case the $\overline{\text{HOLD}}$ pin transited to "L" level when SCK is "H" level, return the $\overline{\text{HOLD}}$ pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{\text{CS}}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	– 0.5	+ 4.0	V
Input voltage*	V_{IN}	– 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output voltage*	V_{OUT}	– 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation ambient temperature	T_A	– 40	+ 85	°C
Storage temperature	Tstg	– 55	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage[*1]	V_{DD}	1.7	3.3	3.6	V
Operation ambient temperature[*2]	T_A	– 40	—	+ 85	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current*[1]	$\lvert I_{LI} \rvert$	$0 \le \overline{\text{CS}} < V_{DD}$	—	—	200	µA
		$\overline{\text{CS}} = V_{DD}$	—	—	1	
		$\overline{\text{WP}}$, $\overline{\text{HOLD}}$, SCK SI = 0 V to V_{DD}	—	—	1	
Output leakage current*[2]	$\lvert I_{LO} \rvert$	SO = 0 V to V_{DD}	—	—	1	µA
Operating power supply current	I_{DD}	SCK = 1MHz	—	0.16	—	mA
		SCK = 33 MHz	—	1.6	2.0	
		SCK = 40 MHz	—	1.9	2.3	
Standby current	I_{SB}	SCK = SI = $\overline{\text{CS}} = V_{DD}$	—	—	50	µA
Sleep current	I_{ZZ}	$\overline{\text{CS}} = V_{DD}$ All inputs V_{SS} or V_{DD}	—	—	10	µA
Input high voltage	V_{IH}	V_{DD} = 1.7 V to 3.6 V	$V_{DD} \times 0.7$	—	$V_{DD} + 0.5$	V
Input low voltage	V_{IL}	V_{DD} = 1.7 V to 3.6 V	− 0.5	—	$V_{DD} \times 0.3$	V
Output high voltage	V_{OH}	I_{OH} = − 2 mA	$V_{DD} - 0.5$	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
Pull up resistance for $\overline{\text{CS}}$	R_P	—	18	33	80	kΩ

*1 : Applicable pin : $\overline{\text{CS}}$, $\overline{\text{WP}}$, $\overline{\text{HOLD}}$, SCK, SI

*2 : Applicable pin : SO

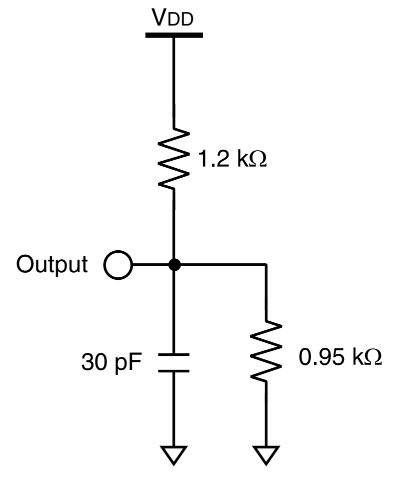
2. AC Characteristics

Parameter	Symbol	Value				Unit
		V_{DD} = 1.7 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		
		Min	Max	Min	Max	
SCK clock frequency	f_{CK}	0	33	0	40	MHz
Clock high time	t_{CH}	13	—	11	—	ns
Clock low time	t_{CL}	13	—	11	—	ns
Chip select set up time	t_{CSU}	10	—	10	—	ns
Chip select hold time	t_{CSH}	10	—	10	—	ns
Output disable time	t_{OD}	—	12	-	12	ns
Output data valid time	t_{ODV}	—	13	-	9	ns
Output hold time	t_{OH}	0	—	0	—	ns
Deselect time	t_D	40	—	40	—	ns
Data in rising time	t_R	—	50	-	50	ns
Data falling time	t_F	—	50	-	50	ns
Data set up time	t_{SU}	5	—	5	—	ns
Data hold time	t_H	5	—	5	—	ns
HOLD set uptime	t_{HS}	10	—	10	—	ns
HOLD hold time	t_{HH}	10	—	10	—	ns
HOLD output floating time	t_{HZ}	—	20	—	20	ns
HOLD output active time	t_{LZ}	—	20	—	20	ns
SLEEP recovery time	t_{REC}	—	400	—	400	µs

AC Test Condition

Power supply voltage : 1.7 V to 3.6 V
Operation ambient temperature : − 40 °C to + 85 °C
Input voltage magnitude : $V_{DD} \times 0.7 \leq V_{IH} \leq V_{DD}$
$0 \leq V_{IL} \leq V_{DD} \times 0.3$
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit

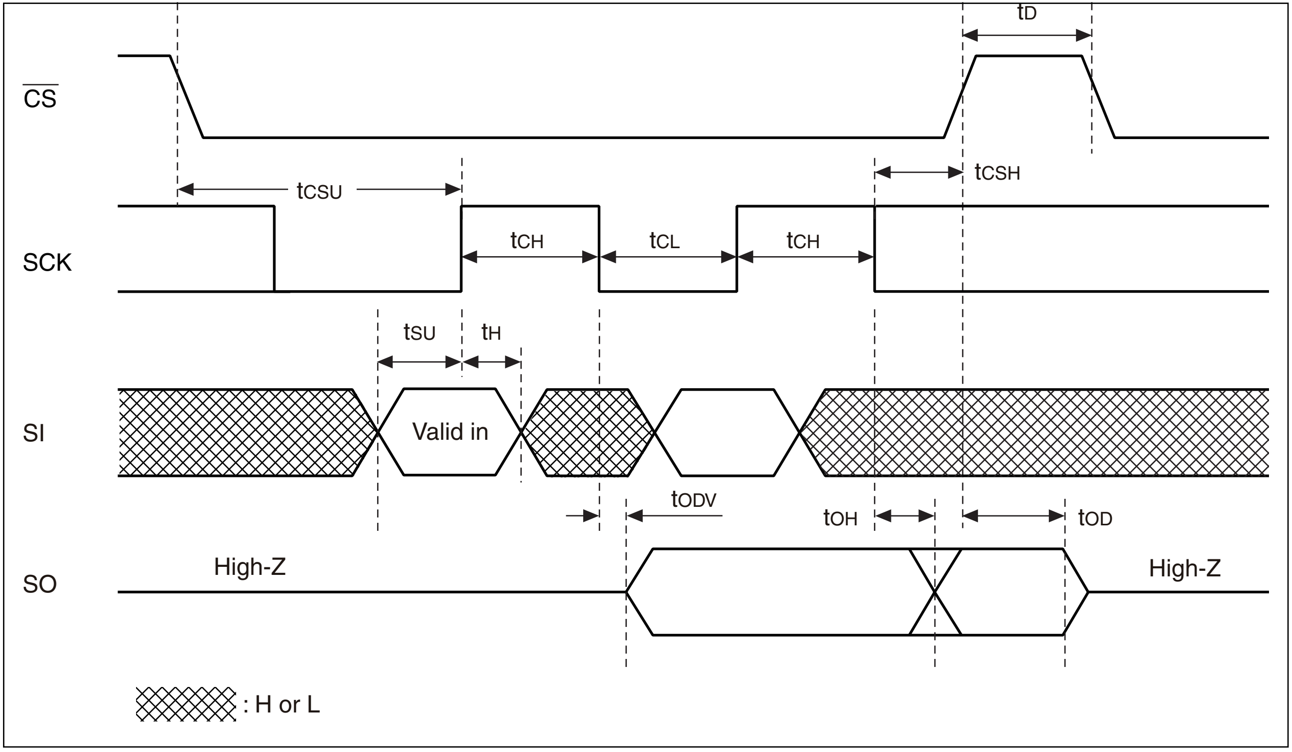

VDD
1.2 kΩ
Output
30 pF
0.95 kΩ

3. Pin Capacitance

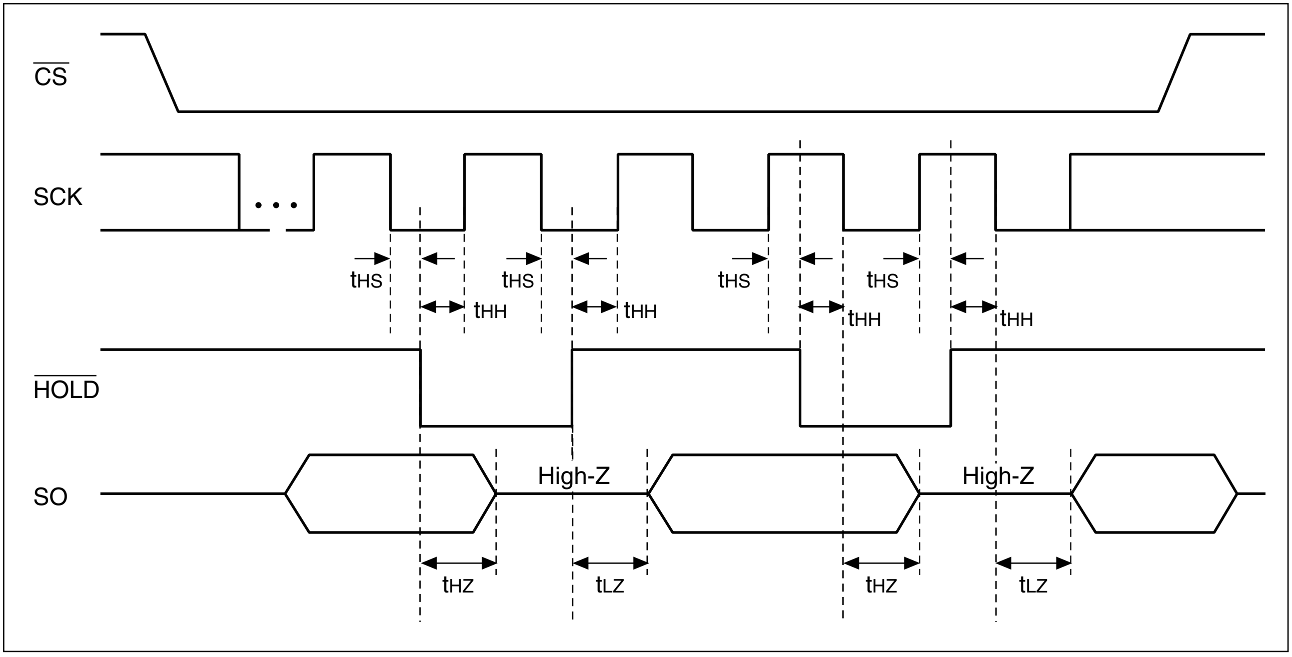
Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_O	$V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A = +25$ °C	—	8	pF
Input capacitance	C_I		—	6	pF

■ TIMING DIAGRAM

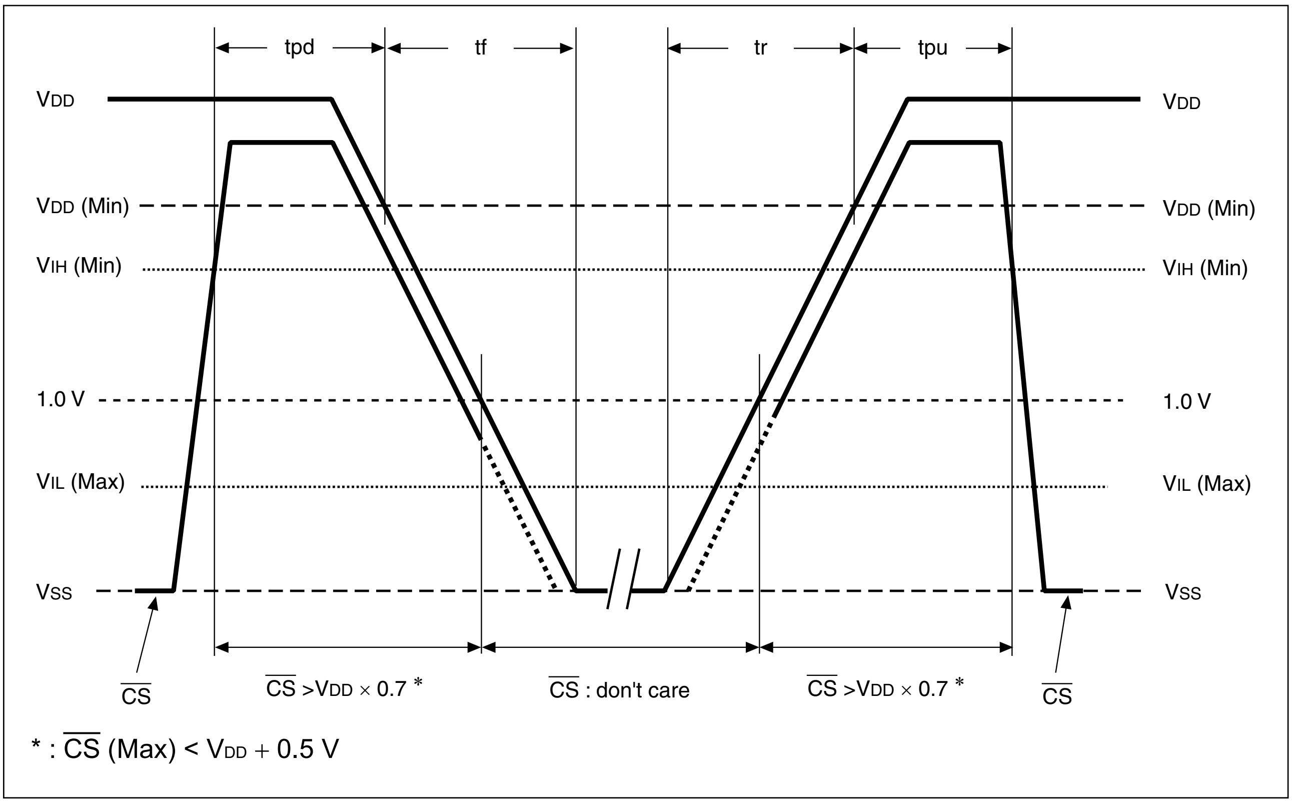
- **Serial Data Timing**


tD
CS
tCSU
tCSH
SCK
tCH
tCL
tCH
tSU
tH
SI
Valid in
tODV
tOH
tOD
SO
High-Z
High-Z
: H or L

- **Hold Timing**


CS
SCK
tHS
tHS
tHS
tHS
tHH
tHH
tHH
tHH
HOLD
SO
High-Z
High-Z
tHZ
tLZ
tHZ
tLZ

■ POWER ON/OFF SEQUENCE


tpd
tf
tr
tpu
VDD
VDD
VDD (Min)
VDD (Min)
VIH (Min)
VIH (Min)
1.0 V
1.0 V
VIL (Max)
VIL (Max)
VSS
VSS
CS
CS >VDD × 0.7 *
CS : don't care
CS >VDD × 0.7 *
CS
* : CS (Max) < VDD + 0.5 V

Parameter	Symbol	Value		Unit	Parameters
		Min	Max		
$\overline{\text{CS}}$ level hold time at power OFF	tpd	0	—	ns	V_{DD} = 2.7V to 3.6V
		400	—		V_{DD} = 1.7V to 2.7V
$\overline{\text{CS}}$ level hold time at power ON	tpu	250	—	µs	
Power supply rising time	tr	0.05	—	ms/V	
Power supply falling time	tf	0.1	—	ms/V	

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance	10^{14}	—	Times	Operation Ambient Temperature T_A = + 85 °C
Data Retention	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C

*1: For details on the Read/Write endurance value, please refer to "■Read/Write endurance about FeRAM".

*2: Minimum values define retention time of the first reading/writing data right after shipment, and the these values are calculated by qualification results.

■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ Read/Write endurance about FeRAM

The value for Read/Write endurance apply to the total number of read and write operations per row in FeRAM. This is because FeRAM needs writing operation after each reading operations.Each row in the memory array has 32 internal outputs, and 8 outputs are selected by A0 and A1. In continuous Read/Write operations, after selecting a certain address and automatically incrementing until A0 and A1 change from (0,0) to (1,1), the Read/Write count endurance count is totaled as one operation. Subsequently, when incrementing automatically and switching to the next row, each row is counted as a new Read/Write operation. If /CS is raised and then the same row is selected again, it is counted as the second operation for that row.

As an actual usage example, if you loop through and access only a memory area (64 bytes or 256 bytes) specified by a specific address in the entire memory area, the number of years it will take to reach 10^{14} times is as below.

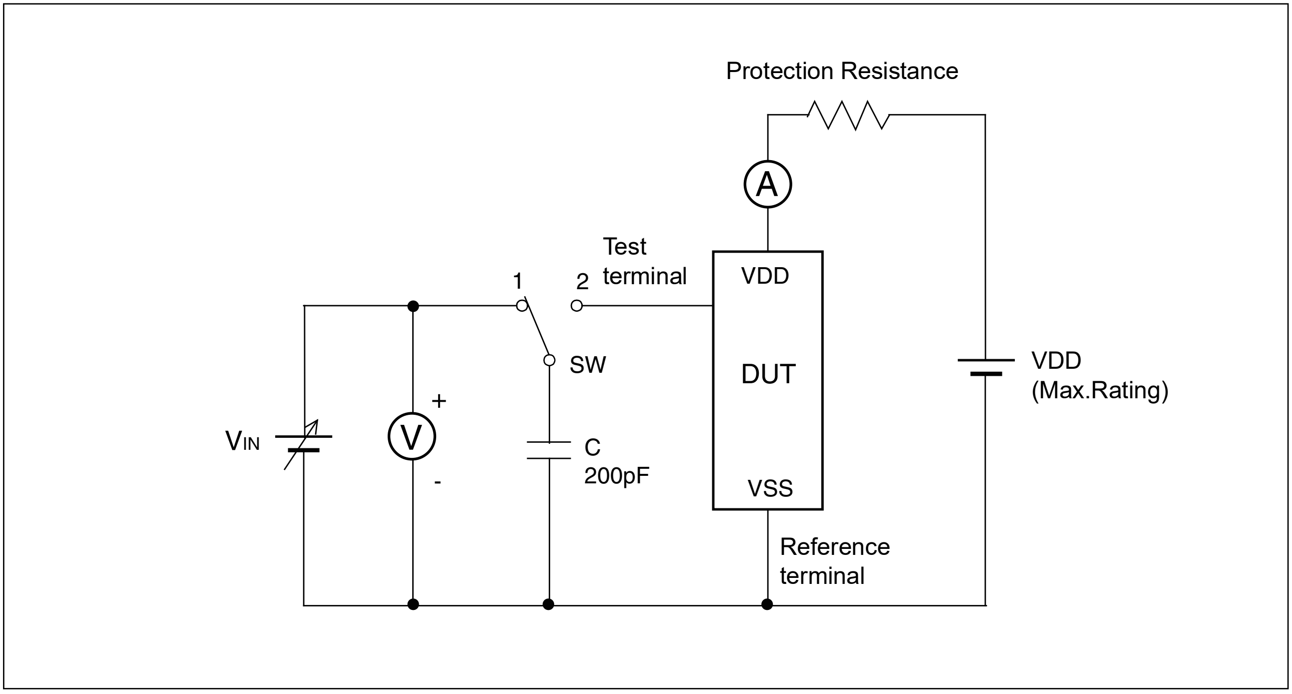
As shown here, with a write endurance of 10^{14} times, even in extreme cases there is enough time before the upper limit is reached, and under normal conditions of use it can be used without worrying about the number of writes/reads.

Operating frequency	Years reached when looping continuously through 64 byte area	Years reached when looping continuously through 256 byte area
40MHz	42.6	164
20MHz	85.1	328
10MHz	170.0	657

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85RS2MTAPNF-G-BDE1 MB85RS2MTAPNF-G-BDERE1 MB85RS2MTAPNF-G-AWE2 MB85RS2MTAPNF-G-AWERE2 MB85RS2MTAPF-G-BCE1 MB85RS2MTAPF-G-BCERE1	≥ |2000 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		≥ |1000 V|
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ MB85RS2MTAPNF/MB85RS2MTAPF (8-pin plastic SOP) REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

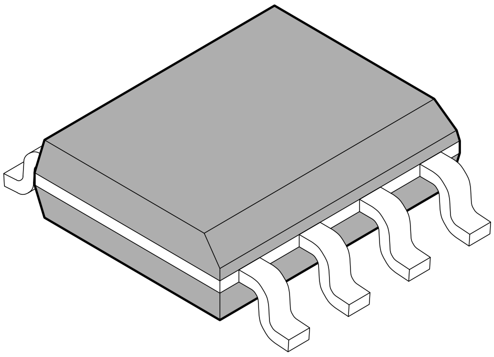
■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS2MTAPNF-G-BDE1	8-pin plastic SOP (150mil)	Tube	— *
MB85RS2MTAPNF-G-BDERE1	8-pin plastic SOP (150mil)	Embossed Carrier tape	1500
MB85RS2MTAPNF-G-AWE2	8-pin plastic SOP (150mil)	Tube	— *
MB85RS2MTAPNF-G-AWERE2	8-pin plastic SOP (150mil)	Embossed Carrier tape	1500
MB85RS2MTAPF-G-BCE1	8-pin plastic SOP (208mil)	Tube	— *
MB85RS2MTAPF-G-BCERE1	8-pin plastic SOP (208mil)	Embossed Carrier tape	500

* : Please contact our sales office about minimum shipping quantity.

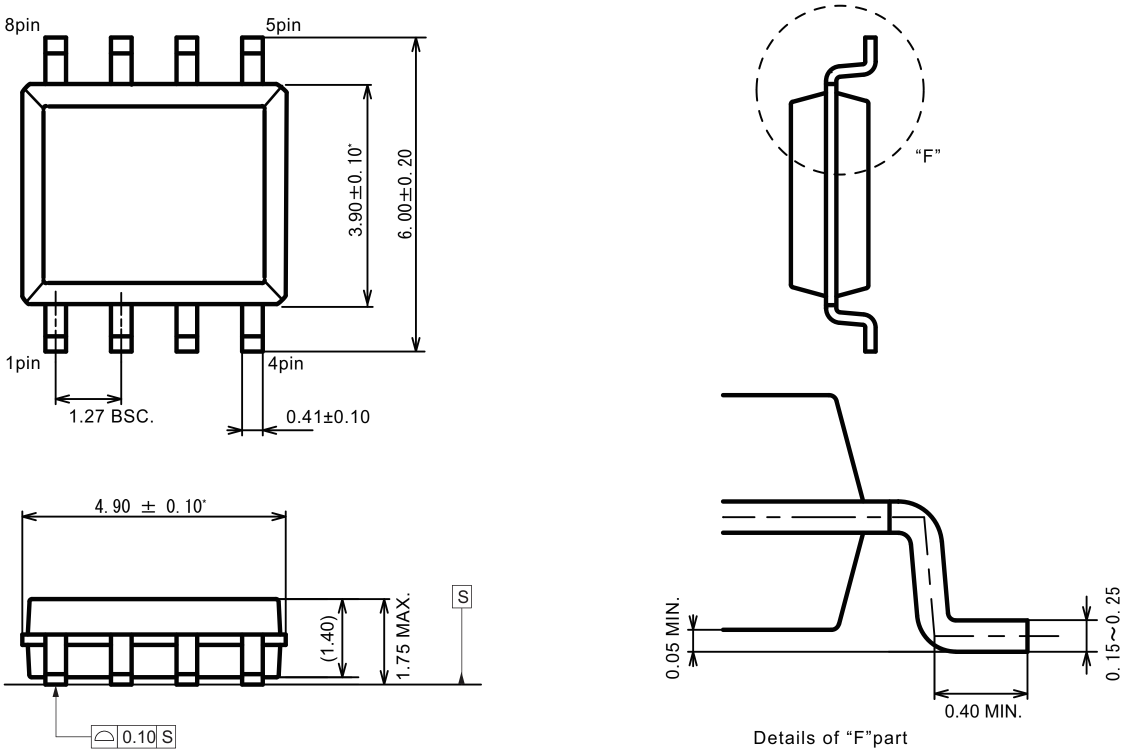
■ PACKAGE DIMENSION

(1)MB85RS2MTAPNF-G-BDE1/MB85RS2MTAPNF-G-BDERE1
MB85RS2MTAPNF-G-AWE2MB85RS2MTAPNF-G-AWERE2

8-pin plastic SOP(150mil) 	Lead pitch	1.27mm
	Package width x Package length	3.90mm x 4.90mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75mm MAX.

8-pin plastic SOP

Note *: These dimension do not include resin protrution.
Pins width do not include tie bar cutting remaindar.


8pin
5pin
1pin
4pin
3.90±0.10*
6.00±0.20
1.27 BSC.
0.41±0.10
4.90 ± 0.10*
(1.40)
1.75 MAX.
S
0.10 S
"F"
0.05 MIN.
0.15~0.25
0.40 MIN.

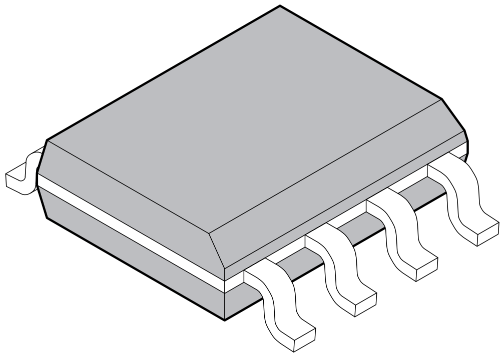
Details of "F"part

Dimension in mm

(continued)

(2)MB85RS2MTAPF-G-BCE1/MB85RS2MTAPF-G-BCERE1

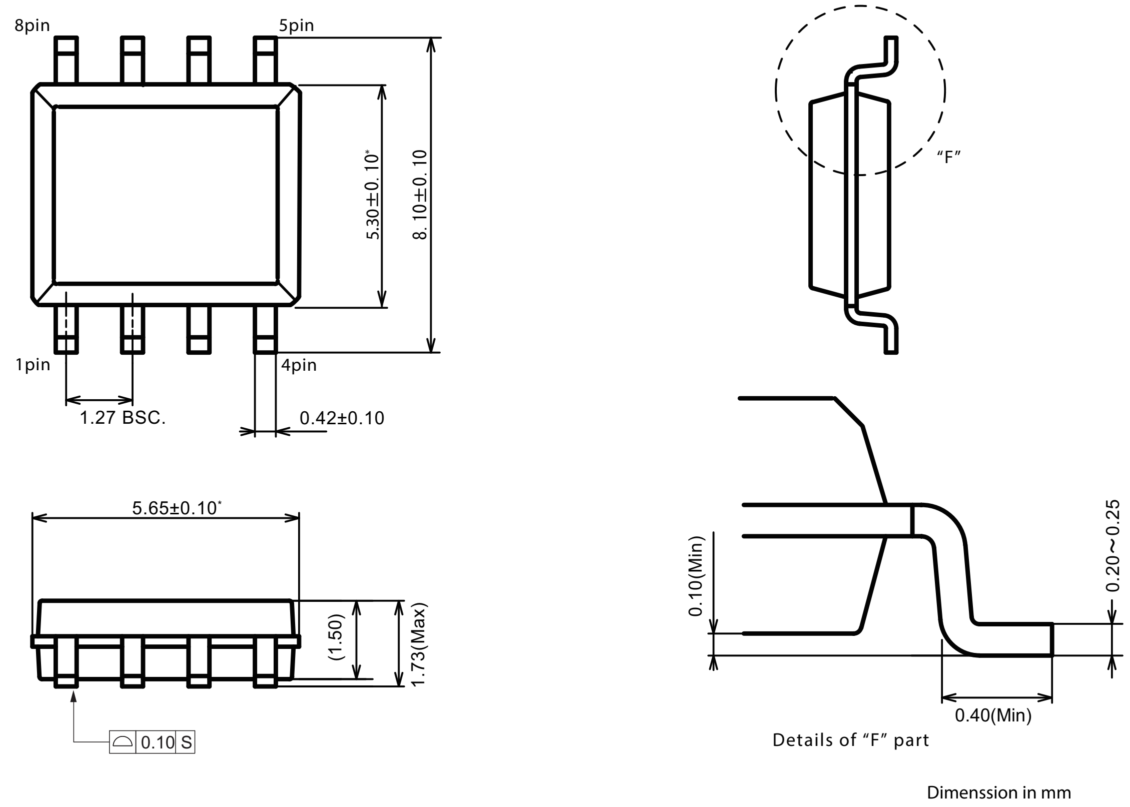
8-pin plastic SOP (208mil)



Lead pitch	1.27 mm
Package width × package length	5.30 mm × 5.65 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting heigth	1.73 mm MAX

8-pin plastic SOP (208mil)

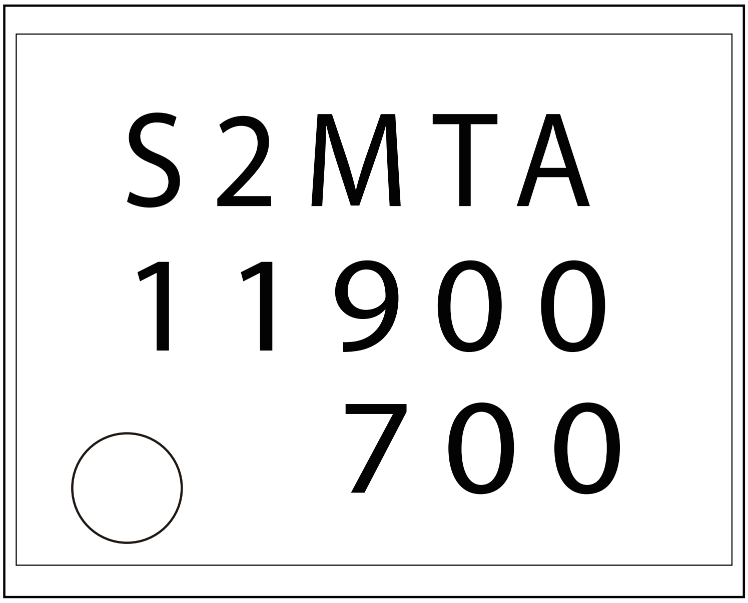
Note *: These dimensions do not include resin protrution.
Pins width not do ninclude tie bar cutting remaindar.


8pin
5pin
5.30±0.10*
8.10±0.10
1pin
4pin
1.27 BSC.
0.42±0.10
5.65±0.10*
(1.50)
1.73(Max)
0.10 S
"F"
0.10(Min)
0.20~0.25
0.40(Min)
Details of "F" part

Dimenssion in mm

■ MARKING

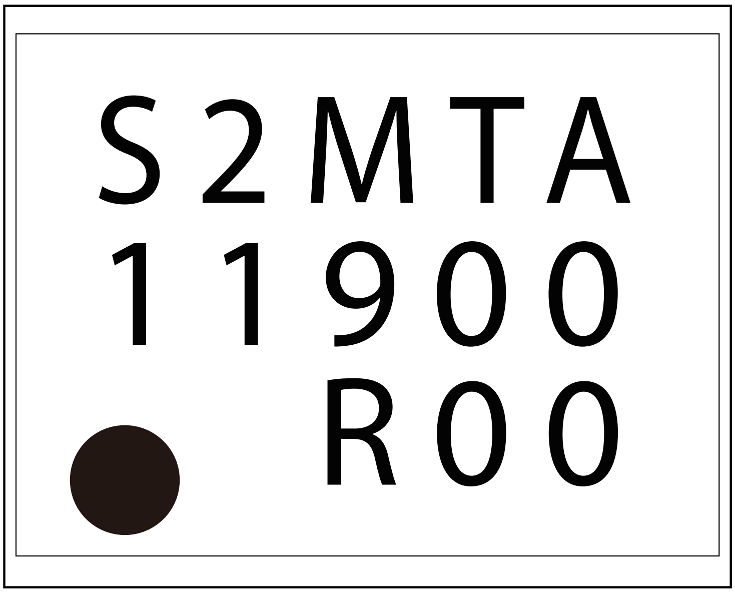
[MB85RS2MTAPNF-G-BDE1]
[MB85RS2MTAPNF-G-BDERE1]



[8-pin plastic SOP, 150mil]

S2MTA: Product Name
11900: 1 (CS code) + 1900(Year and Week code)
700: Trace code

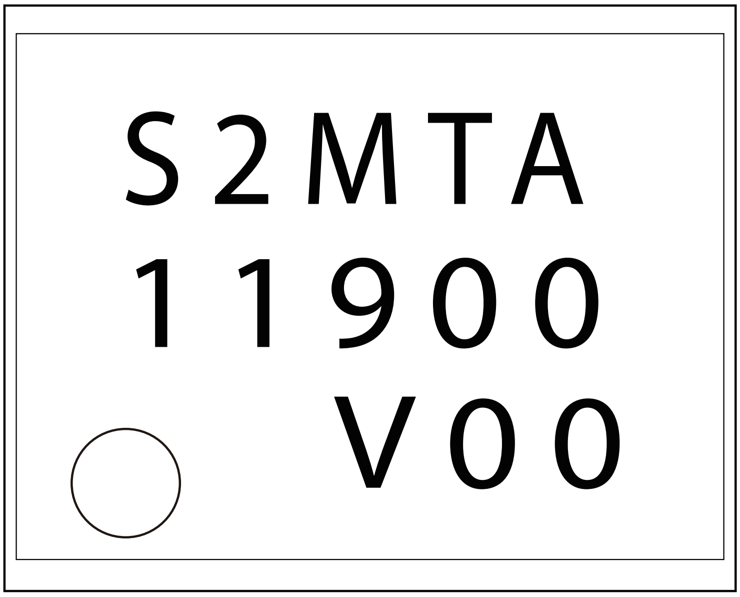
[MB85RS2MTAPNF-G-AWE2]
[MB85RS2MTAPNF-G-AWERE2]



[8-pin plastic SOP, 150mil]

S2MTA: Product Name
11900: 1 (CS code) + 1900(Year and Week code)
R00: Trace code

[MB85RS2MTAPF-G-BCE1]
[MB85RS2MTAPF-G-BCERE1]



[8-pin plastic SOP, 208mil]

S2MTA: Product Name
11900: 1 (CS code) + 1900(Year and Week code)
V00: Trace code

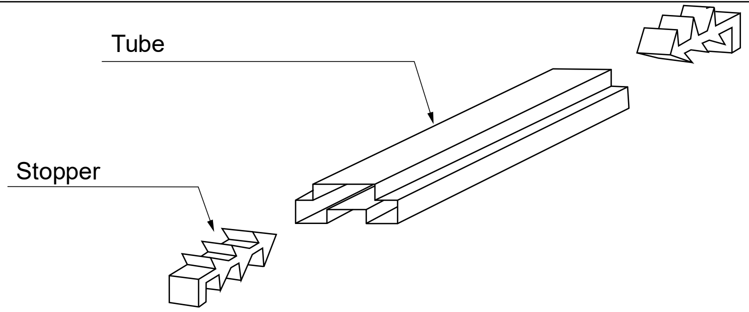
■ PACKING INFORMATION

(1)MB85RS2MTAPNF-G-BDE1/MB85RS2MTAPNF-G-BDERE1/ MB85RS2MTAPNF-G-AWE2/MB85RS2MTAPNF-G-AWERE2 (8-pin plastic SOP, 150mil)

1. **Tube** (MB85RS2MTAPNF-G-BDE1/MB85RS2MTAPNF-G-AWE2)

1.1 Tube Dimensions

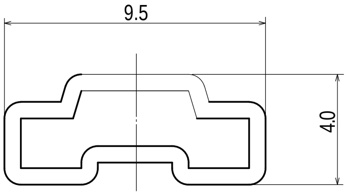
- Tube/stopper shape (example)



- **Tube cross-sections** and Maximum quantity

MB85RS2MTAPNF-G-BDE1

Maximum quantity		
ICs/tube	ICs/inner box	ICs/outer box
85	4,250	17,000



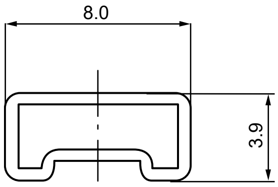
No heat resistance.
Package should not be baked by using tape and reel.

tube length: 500

(Dimensions in mm)

MB85RS2MTAPNF-G-AWE2

Maximum quantity		
ICs/tube	ICs/inner box	ICs/outer box
85	4,250	25,500

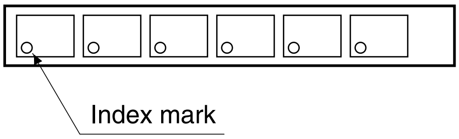


No heat resistance.
Package should not be baked by using tape and reel.

tube length: 509

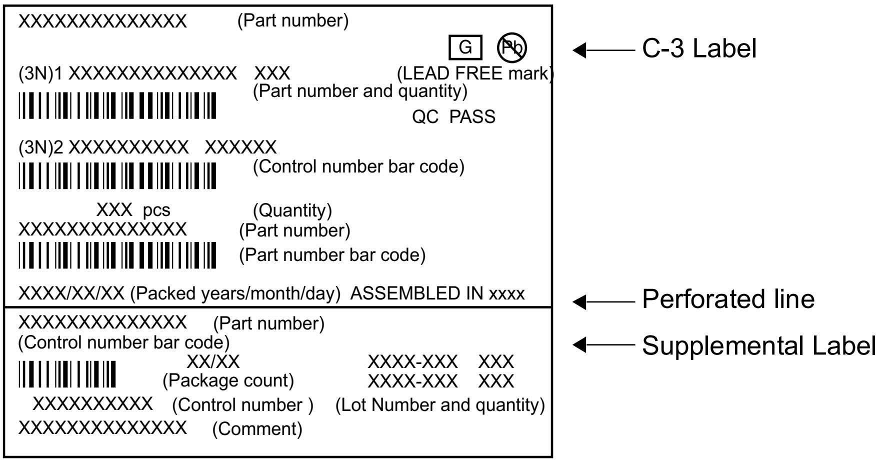
(Dimensions in mm)

- Tube orientation



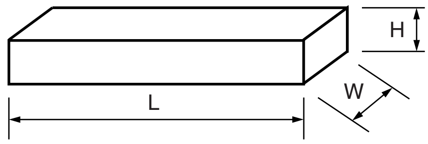
1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs
(Quantity)
XXXXXXXXXXXXXX
(Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

1.3 Dimensions for Containers

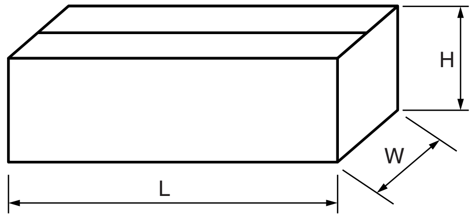
(1) Dimensions for inner box



Part number	L	W	H
MB85RS2MTAPNF-G-BDE1	540	125	75
MB85RS2MTAPNF-G-AWE2	549	125	81

(Dimensions in mm)

(2) Dimensions for outer box



Part number	L	W	H
MB85RS2MTAPNF-G-BDE1	565	270	180
MB85RS2MTAPNF-G-AWE2	567	272	269

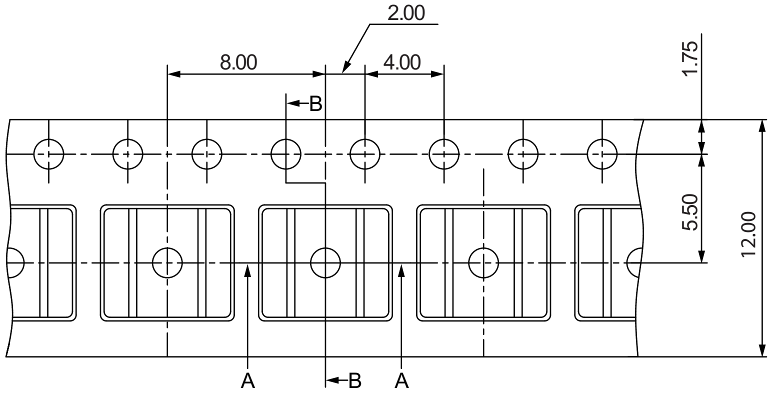
(Dimensions in mm)

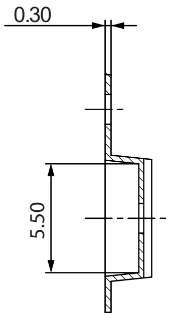
2. **Emboss Tape** (MB85RS2MTAPNF-G-BDERE1/MB85RS2MTAPNF-G-AWERE2)

2.1 **Tape Dimensions** (not drawn to scale)(8-pin plastic SOP, 150mil)

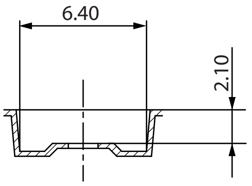
2.1.1 MB85RS2MTAPNF-G-BDERE1

reel diameter (mm)	Maximum storage capacity			MSL Label
	ICs/reel(mm)	ICs/inner box	ICs/outer box	
Φ254	1,500	1,500 (1 pack/inner box)	9,000 (6 inner boxes/ outer box:Max.)	No





SEC.B-B



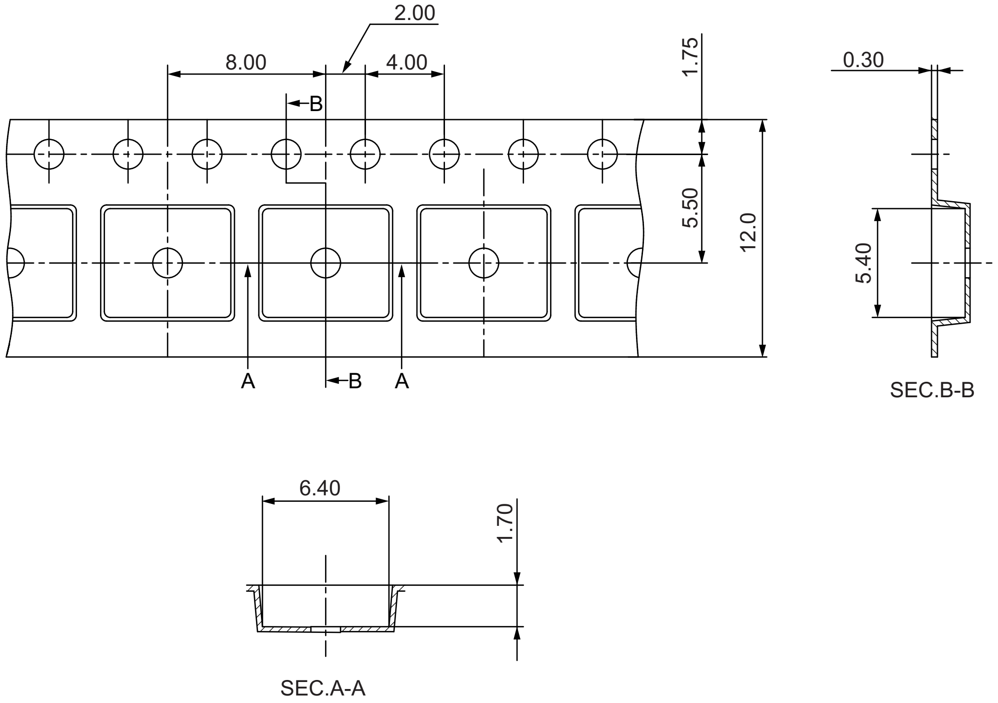
SEC.A-A

(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked
by using tape and reel.

2.1.2 MB85RS2MTAPNF-G-AWERE2

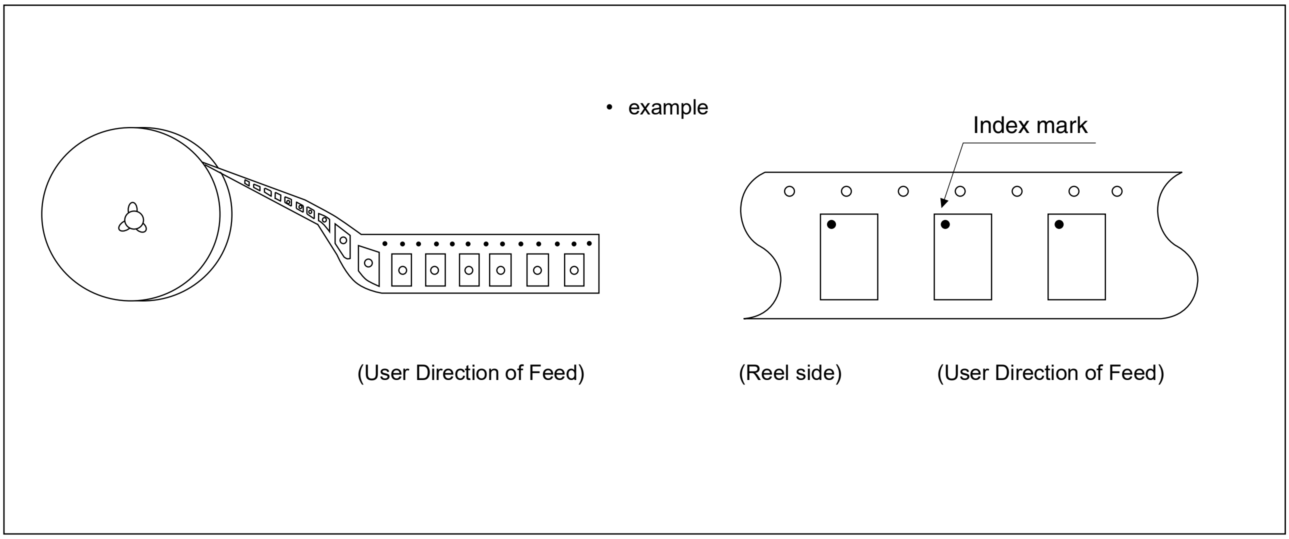
reel diameter (mm)	Maximum storage capacity			MSL Label
	ICs/reel(mm)	ICs/inner box	ICs/outer box	
Φ330	1,500	1,500 (1 pack/inner box)	7,500 (5 inner boxes/ outer box:Max.)	Yes


2.00
8.00
4.00
1.75
0.30
B
5.50
12.0
5.40
A
B
A
SEC.B-B
6.40
1.70
SEC.A-A

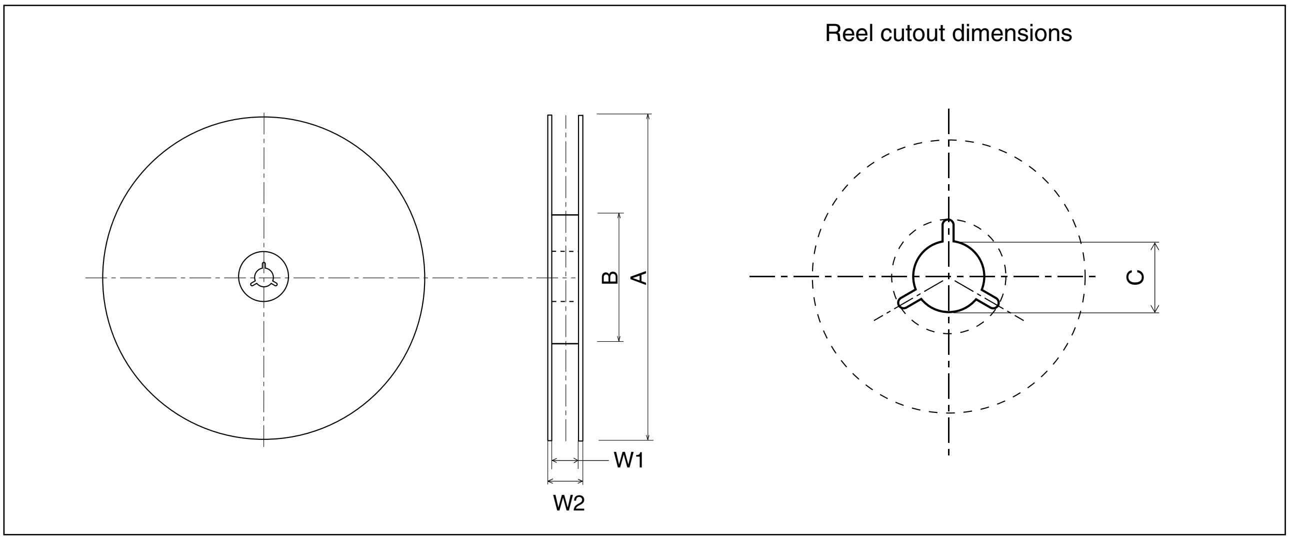
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked
by using tape and reel.

2.2 IC orientation


• example
Index mark
(User Direction of Feed)
(Reel side)
(User Direction of Feed)

2.3 Reel dimensions

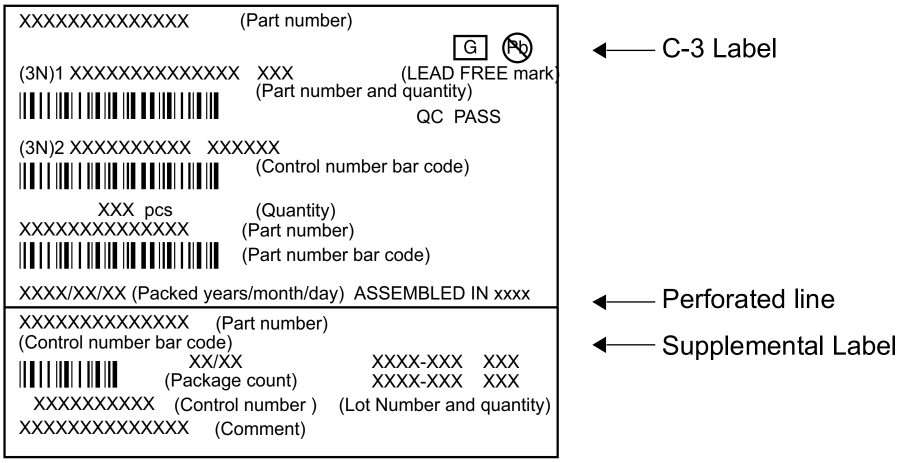

Reel cutout dimensions
B
A
C
W1
W2

Dimensions in mm

Part number	A	B	C	W1	W2
MB85RS2MTAPNF-G-BDERE1	254	100	13	13.5	17.5
MB85RS2MTAPNF-G-AWERE2	330	100	13	13.5	17.5

2.4 Product label indicators (example)

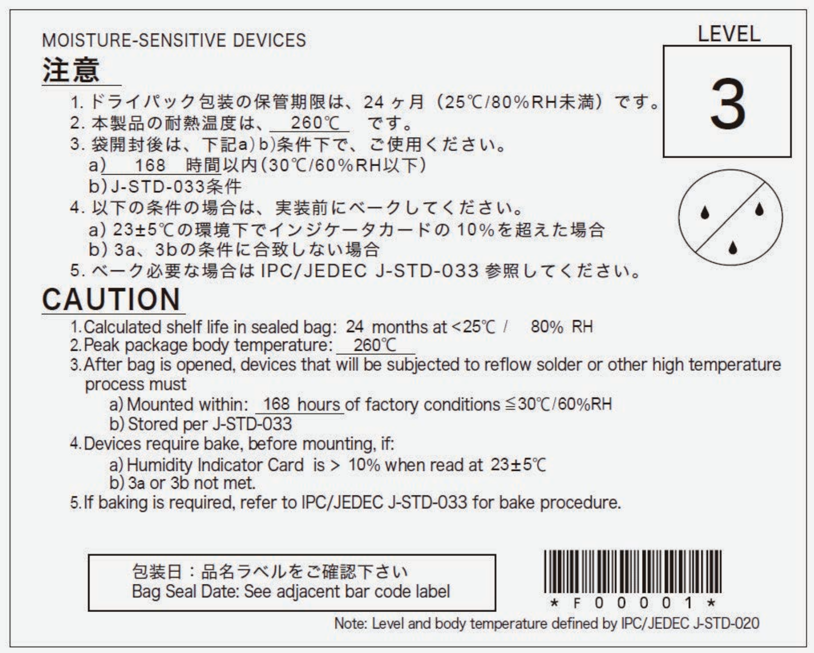
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



XXXXXXXXXXXXXX (Part number)
G
(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx

XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
[MSL Label]



MOISTURE-SENSITIVE DEVICES

LEVEL
3

注意

1. ドライパック包装の保管期限は、24ヶ月（25℃/80%RH未満）です。
2. 本製品の耐熱温度は、 260℃ です。
3. 袋開封後は、下記a）b）条件下で、ご使用ください。
   a） 168 時間以内（30℃/60%RH以下）
   b）J-STD-033条件
4. 以下の条件の場合は、実装前にベークしてください。
   a）23±5℃の環境下でインジケータカードの10%を超えた場合
   b）3a、3bの条件に合致しない場合
5. ベーク必要な場合はIPC/JEDEC J-STD-033参照してください。

CAUTION

1. Calculated shelf life in sealed bag: 24 months at <25℃ / 80% RH
2. Peak package body temperature: 260℃
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 168 hours of factory conditions ≦30℃/60%RH
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is > 10% when read at 23±5℃
   b) 3a or 3b not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

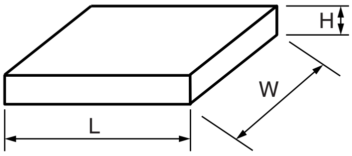
包装日：品名ラベルをご確認下さい
Bag Seal Date: See adjacent bar code label

* F 0 0 0 0 1 *

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

2.5 Dimensions for Containers

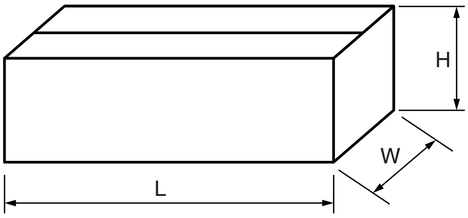
(1) Dimensions for inner box



Part number	L	W	H
MB85RS2MTAPNF-G-BDERE1	265	260	50
MB85RS2MTAPNF-G-AWERE2	350	335	35

(Dimensions in mm)

(2) Dimensions for outer box



Part number	L	W	H
MB85RS2MTAPNF-G-BDERE1	565	270	180
MB85RS2MTAPNF-G-AWERE2	384	368	225

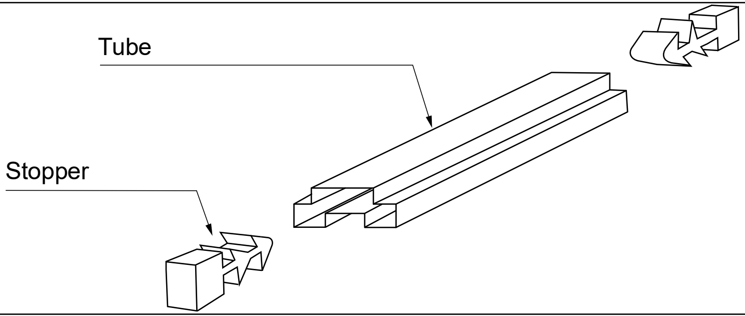
(Dimensions in mm)

(2)MB85RS2MTAPF-G-BCE1/MB85RS2MTAPF-G-BCERE1 (8-pin plastic SOP, 208mil)

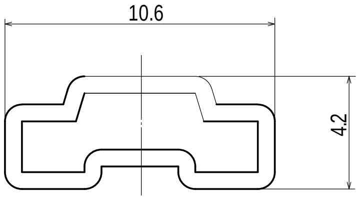
1. Tube (MB85RS2MTAPF-G-BCE1)

1.1Tube Dimensions

- Tube/stopper shape (example))

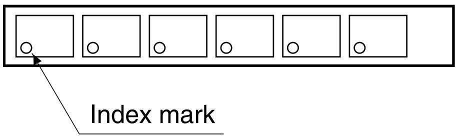


- **Tube cross-sections** and Maximum quantity

Package form	Maximum quantity		
	ICs/tube	ICs/inner box	ICs/outer box
 No heat resistance. Package should not be baked by using tape and reel.	80	4,000 (50 tube/inner box)	16,000 (Max:4 inner box/outer box)
	tube length: 508		

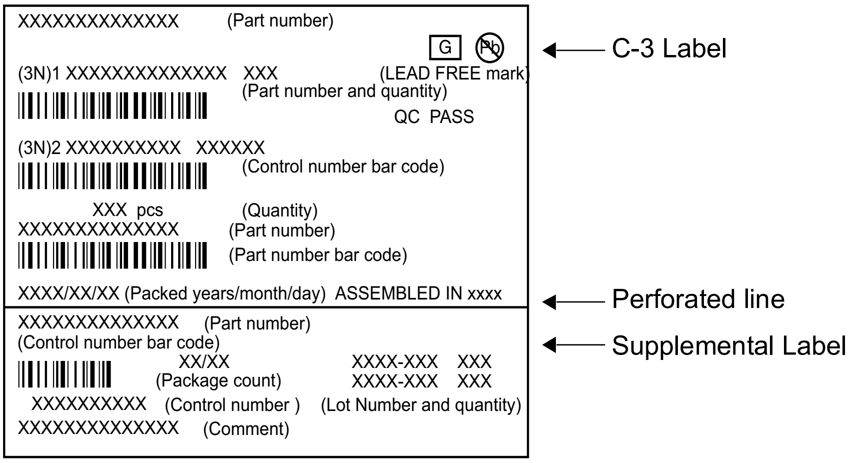
(Dimensions in mm)

- Tube orientation



1.2 Product label indicators (example)

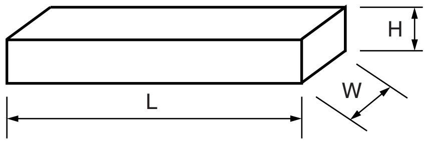
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



XXXXXXXXXXXXXX (Part number)
G Pb
(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number) (Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)

1.3 Dimensions for Containers

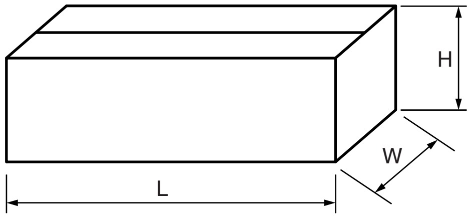
(1) Dimensions for inner box



L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box



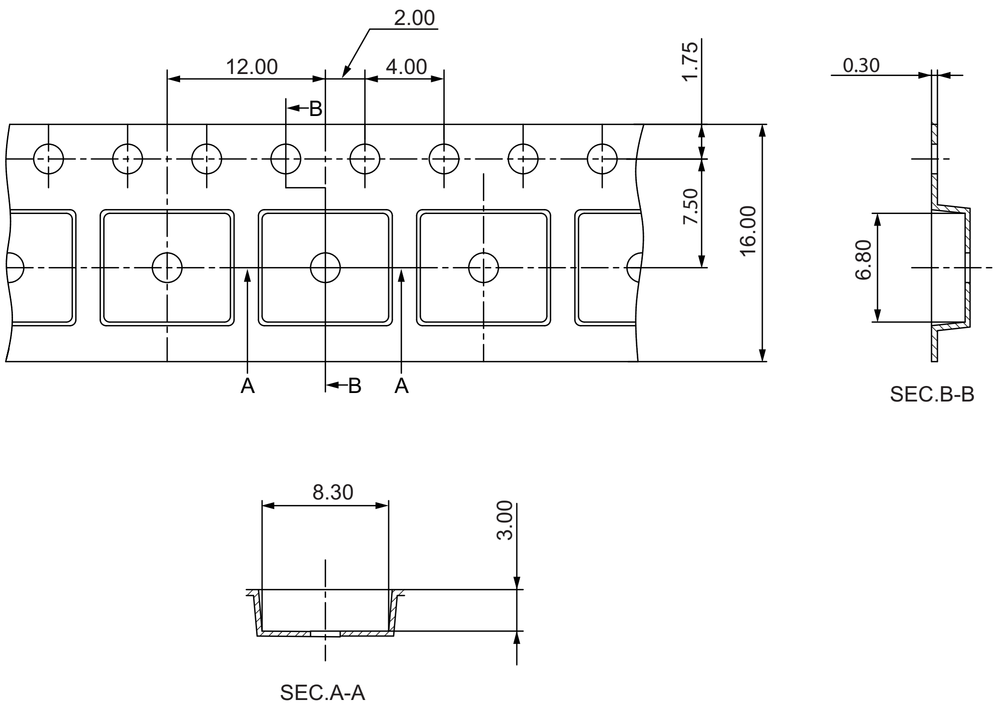
L	W	H
565	270	180

(Dimensions in mm)

2. **Emboss Tape** (MB85RS2MTAPF-G-BCERE1**)**

2.1 **Tape Dimensions** (not drawn to scale)(8-pin plastic SOP, 208mil)

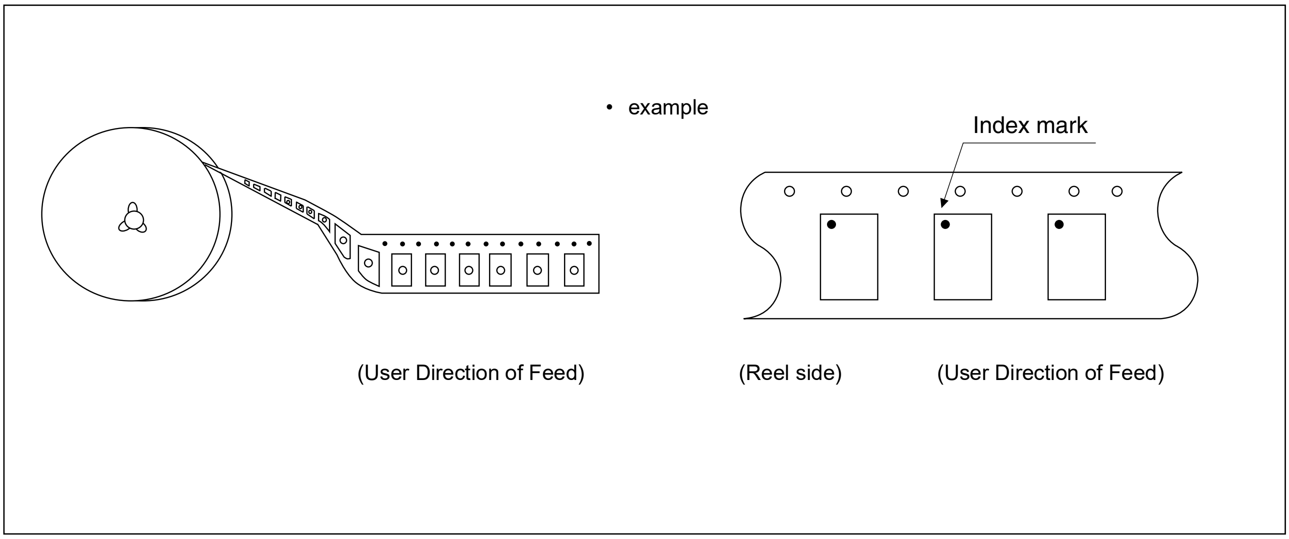
reel diameter (mm)	Maximum storage capacity			MSL Label
	ICs/reel(mm)	ICs/inner box	ICs/outer box	
Φ254	500	500 (1 pack/inner box)	3,000 (6 inner boxes/ outer box:Max.)	Yes


2.00
12.00
4.00
1.75
0.30
B
7.50
16.00
6.80
A
B
A
SEC.B-B
8.30
3.00
SEC.A-A

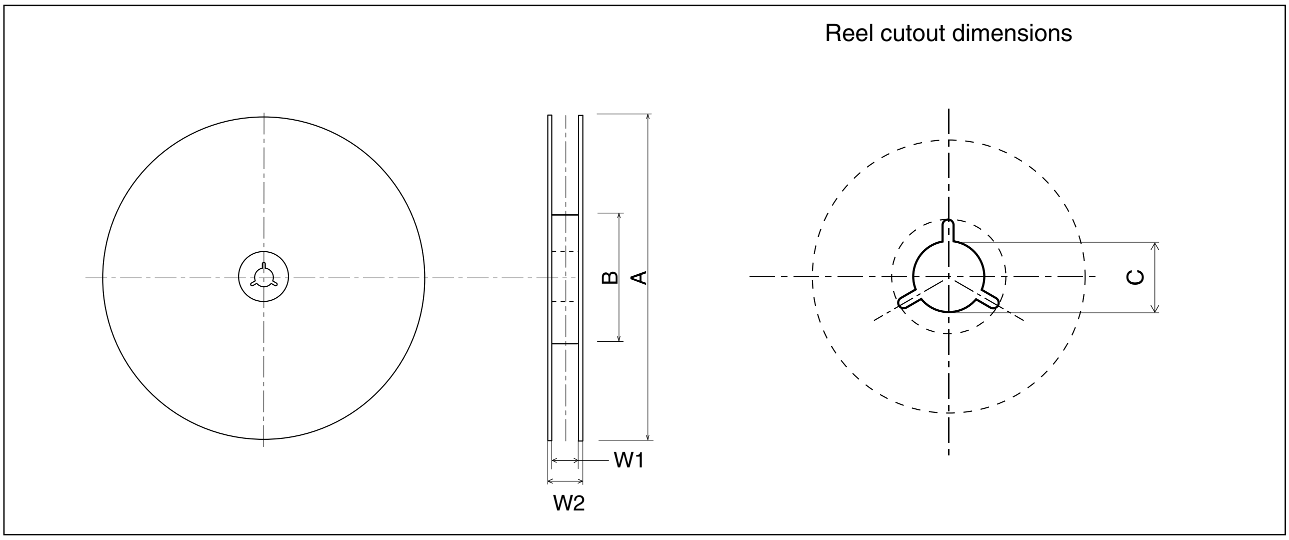
(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked
by using tape and reel.

2.2 IC orientation


• example
Index mark
(User Direction of Feed)
(Reel side)
(User Direction of Feed)

2.3 Reel dimensions

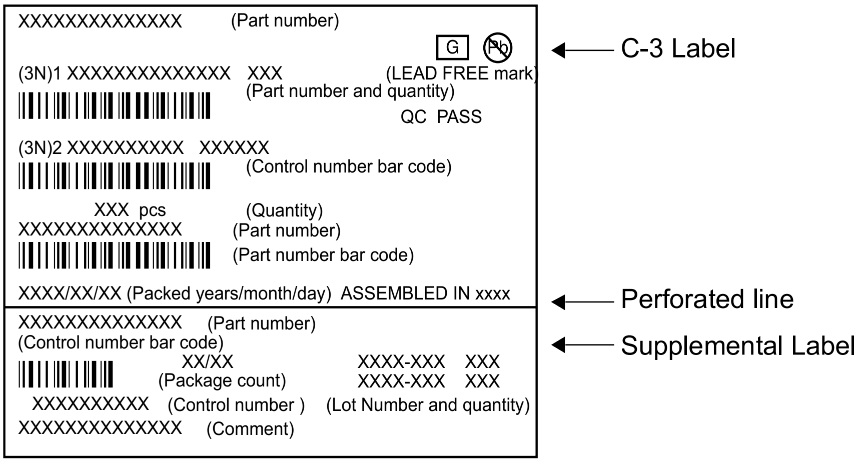

Reel cutout dimensions
B
A
W1
W2
C

Dimensions in mm

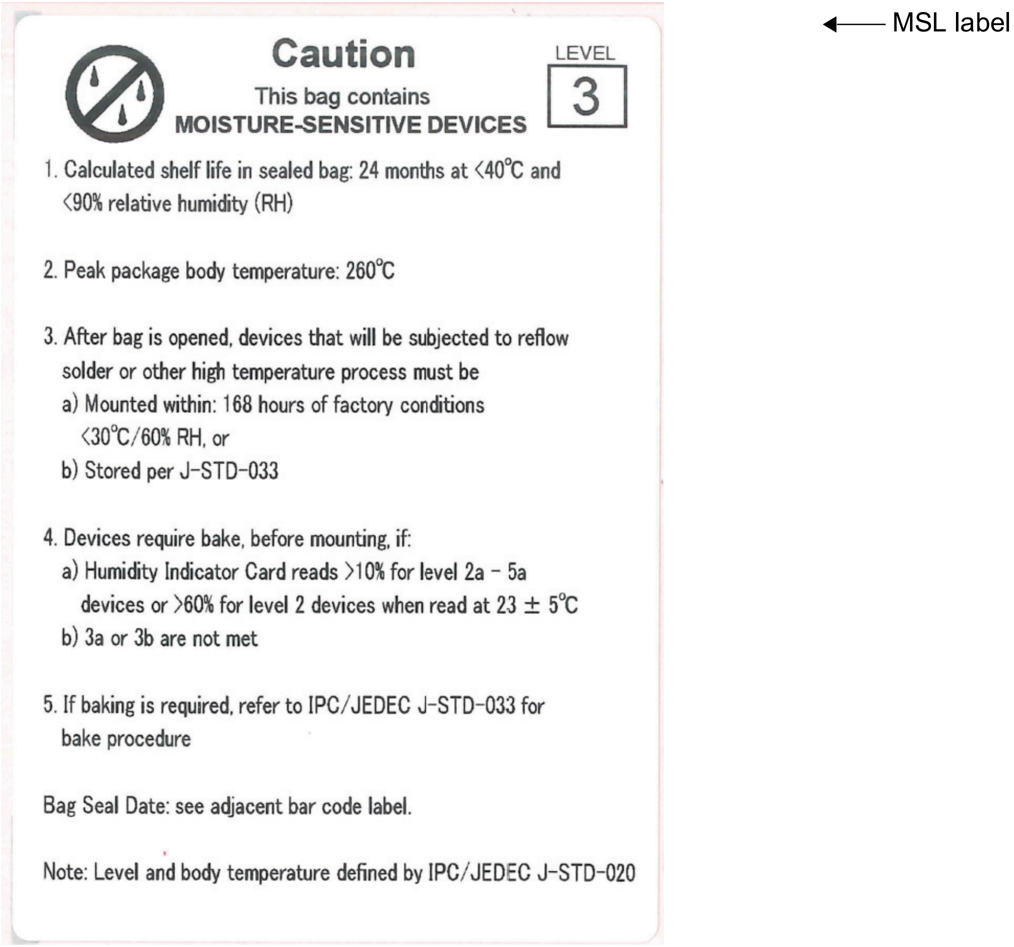
A	B	C	W1	W2
254	100	13	17.5	21.5

2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]


XXXXXXXXXXXXXX (Part number)
G
Pb
(3N)1 XXXXXXXXXXXXXX XXX
(LEAD FREE mark)
(Part number and quantity)
QC PASS
(3N)2 XXXXXXXXXX XXXXXX
(Control number bar code)
XXX pcs (Quantity)
XXXXXXXXXXXXXX (Part number)
(Part number bar code)
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx
XXXXXXXXXXXXXX (Part number)
(Control number bar code)
XX/XX
(Package count)
XXXX-XXX XXX
XXXX-XXX XXX
XXXXXXXXXX (Control number)
(Lot Number and quantity)
XXXXXXXXXXXXXX (Comment)
C-3 Label
Perforated line
Supplemental Label

Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
[MSL Label]



Caution

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
3

1. Calculated shelf life in sealed bag: 24 months at <40°C and <90% relative humidity (RH)

2. Peak package body temperature: 260°C

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: 168 hours of factory conditions <30°C/60% RH, or
   b) Stored per J-STD-033

4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads >10% for level 2a – 5a devices or >60% for level 2 devices when read at 23 ± 5°C
   b) 3a or 3b are not met

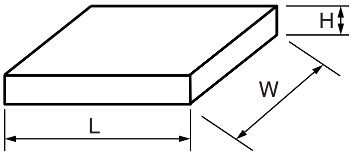
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: see adjacent bar code label.

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

2.5 Dimensions for Containers

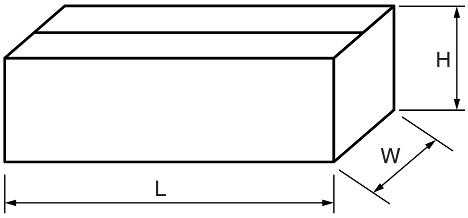
(1) Dimensions for inner box



L	W	H
265	260	50

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
565	270	180

(Dimensions in mm)

■ MAJOR CHANGES IN THIS EDITION

Changes on pages are indicated by vertical lines drawn on the left side of that pages.

Page	Section	Change Results
1,17	High endurance	10^{13}times/byte → 10^{14}times
18	Read/Write endurance about FeRAM	Add information

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