Memory FeRAM

4 M (512 K × 8) Bit SPI

MB85RS4MT

■ DESCRIPTION

MB85RS4MT is a FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 524,288 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

MB85RS4MT adopts the Serial Peripheral Interface (SPI).

The MB85RS4MT is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85RS4MT can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
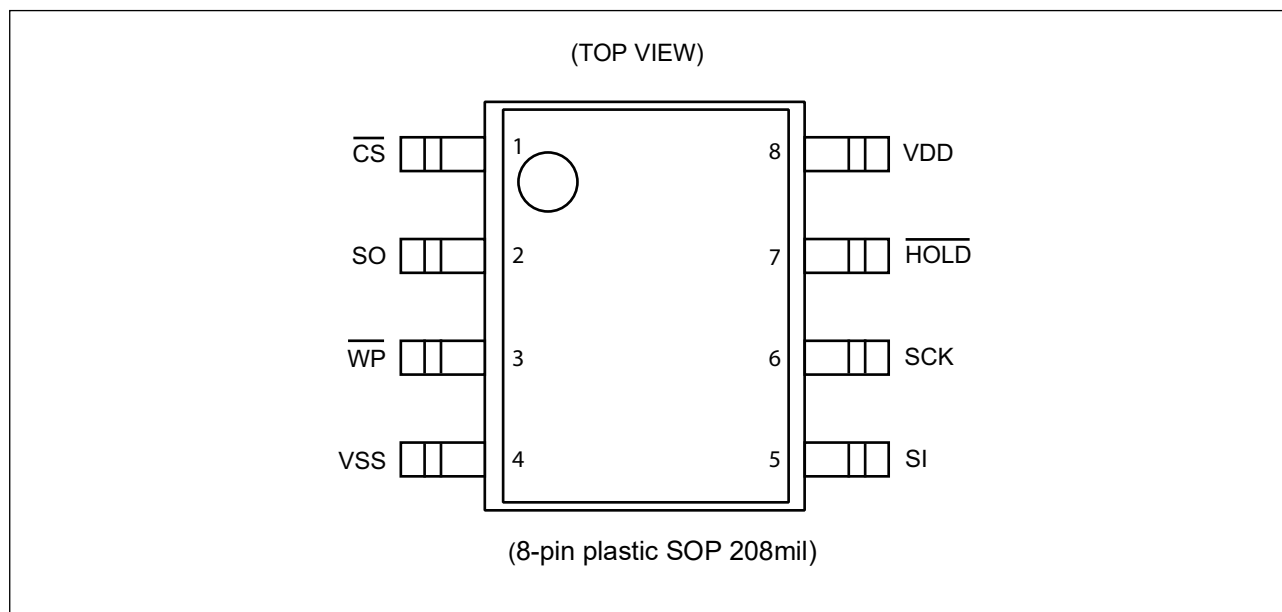
MB85RS4MT does not take long time to write data like Flash memories or E^2PROM, and MB85RS4MT takes no wait time.

■ FEATURES

- Bit configuration : 524,288 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 40MHz (Max)

- High endurance : 10^{14} times
- Data retention : 10 years (+85 °C),95 years(+55 °C), over 200 years(+35 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low power consumption : Operating power supply current 2.6mA (Max@40 MHz)
  Standby current 50 μA (Max)
  Sleep current 8μA (Max)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 8-pin plastic SOP (208mil)
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.
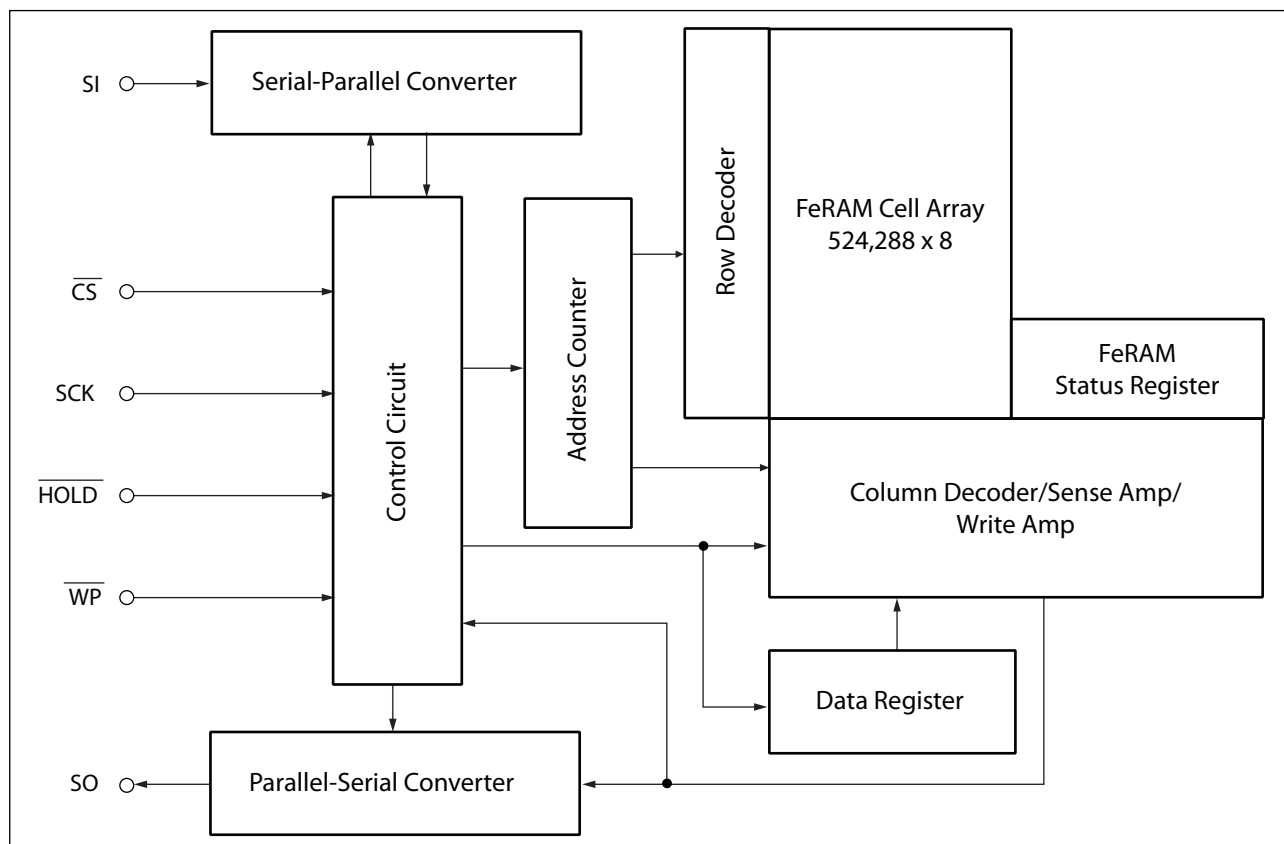
■ PIN ASSIGNMENT

(TOP VIEW)

```
     ___
     CS  [1  ○        8]  VDD
                          ____
     SO  [2           7]  HOLD
     ___
     WP  [3           6]  SCK

     VSS [4           5]  SI
```

(8-pin plastic SOP 208mil)

■ PIN FUNCTIONAL DESCRIPTIONS

| Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is "H" level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is "L" level, device is in select (active) status. $\overline{CS}$ has to be "L" level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. The writing of status register (see "■ STATUS REGISTER") is protected in related with $\overline{WP}$ and WPEN. See "■ WRITING PROTECT" for detail.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. See "■ HOLD OPERATION" for detail.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FeRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	VSS	Ground pin

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■ BLOCK DIAGRAM

■ SPI MODE

MB85RS4MT corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .
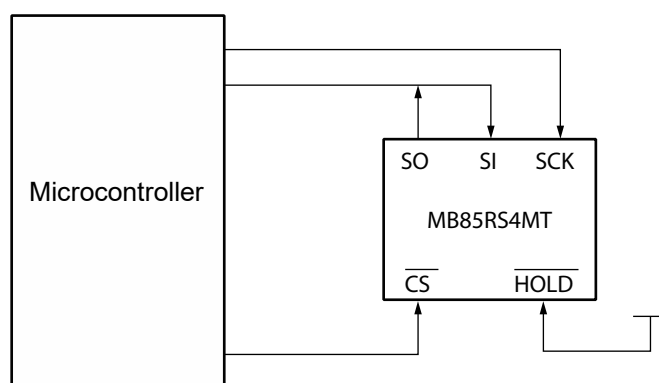

SPI Mode 0

SPI Mode 3
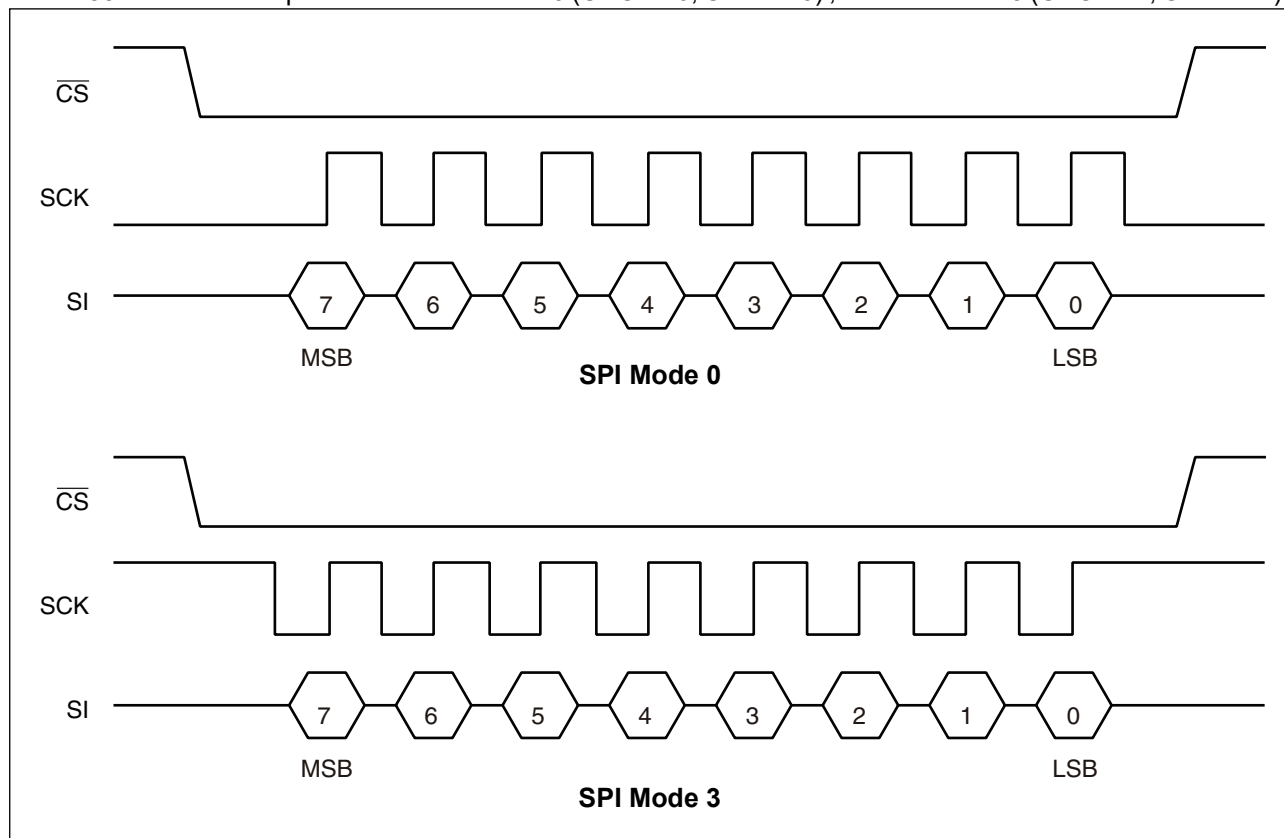
■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS4MT works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.

MOSI : Master Out Slave In
MISO : Master In Slave Out
SS : Slave Select
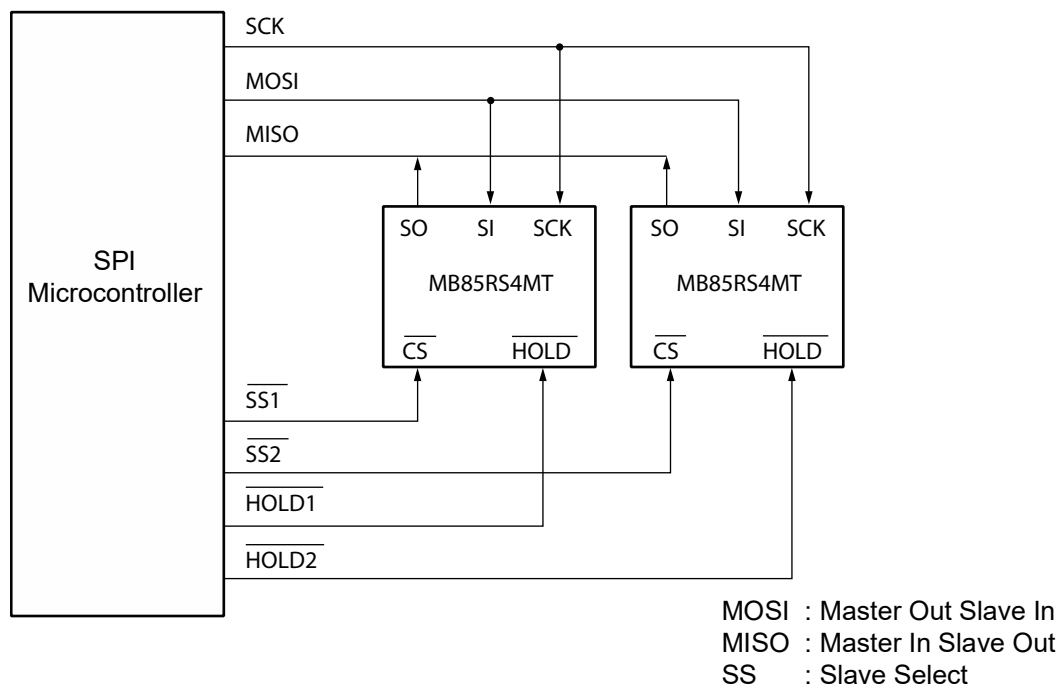
System Configuration with SPI Port

System Configuration without SPI Port

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■ STATUS REGISTER

| Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FeRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	

1	WEL	Write Enable Latch
		This indicates FeRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations.
		    After power ON.
		    After WRDI command recognition.
		    After return from SLEEP mode.
		Achieving continuous writing mode, WEL is not reset after following operations making it possible to execute writing commands continuously.
		    After WRSR command recognition.
		    After WRITE command recognition.

0	0	This is a bit fixed to "0".

■ OP-CODE

MB85RS4MT accepts 9 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

| Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110B
WRDI	Reset Write Enable Latch	0000 0100B
RDSR	Read Status Register	0000 0101B
WRSR	Write Status Register	0000 0001B
READ	Read Memory Code	0000 0011B
WRITE	Write Memory Code	0000 0010B
RDID	Read Device ID	1001 1111B
FSTRD	Fast Read Memory Code	0000 1011B
SLEEP	Sleep Mode	1011 1001B

■ COMMAND

• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .
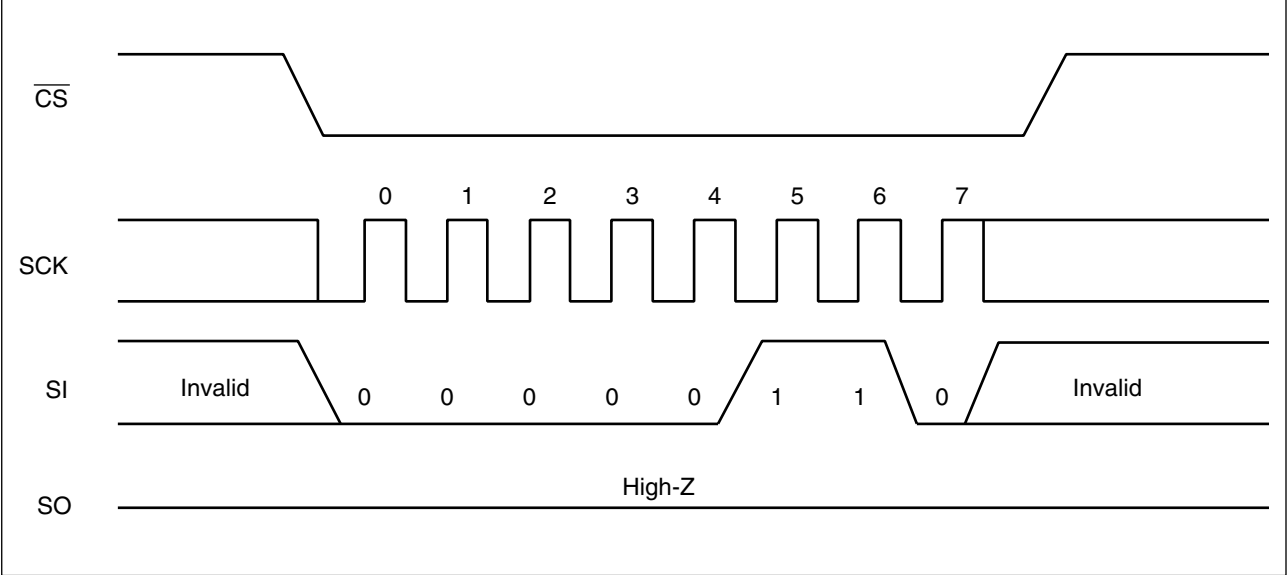

• WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.

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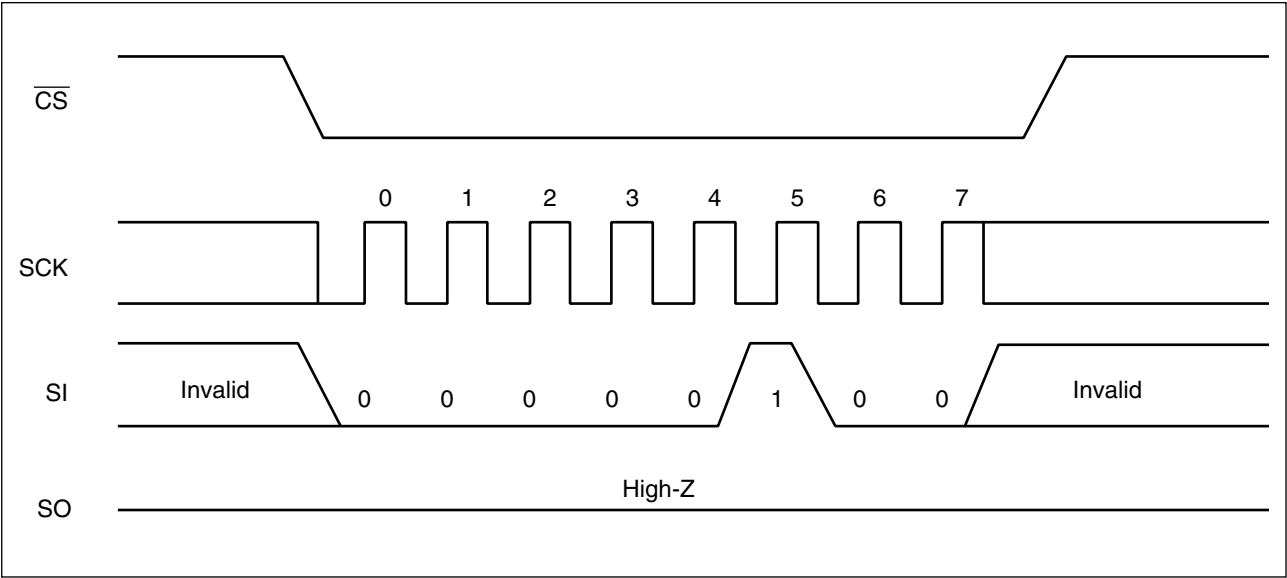
- **RDSR**

    The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.
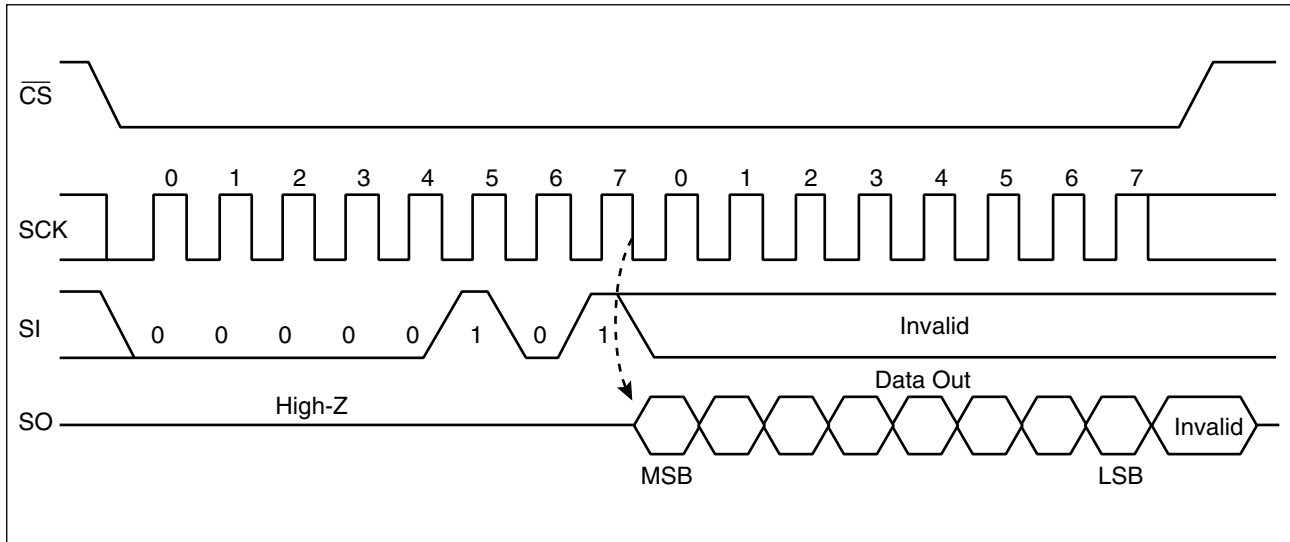

- **WRSR**

    The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{WP}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence.
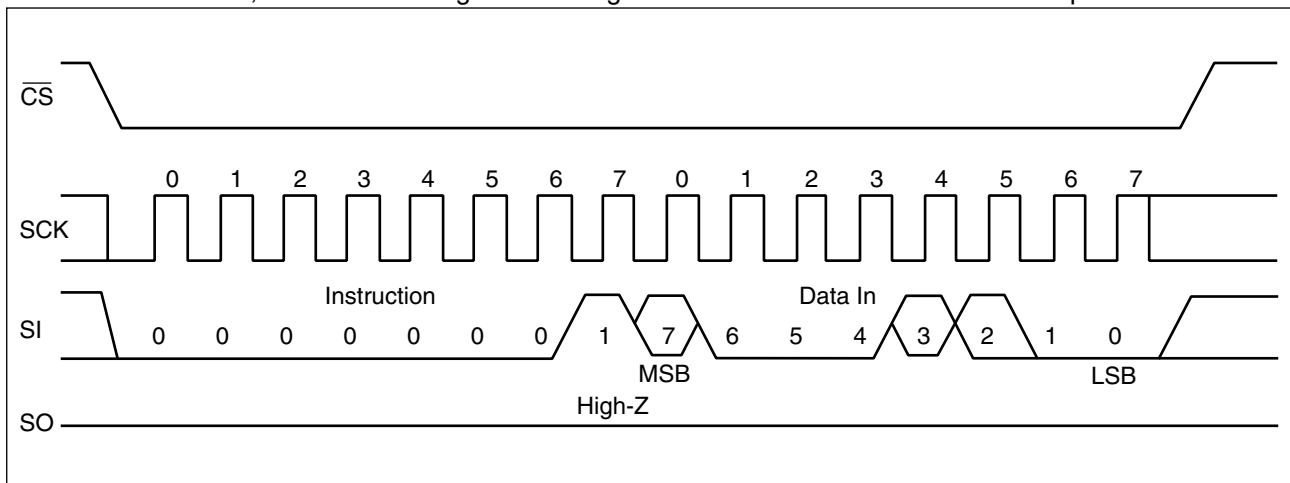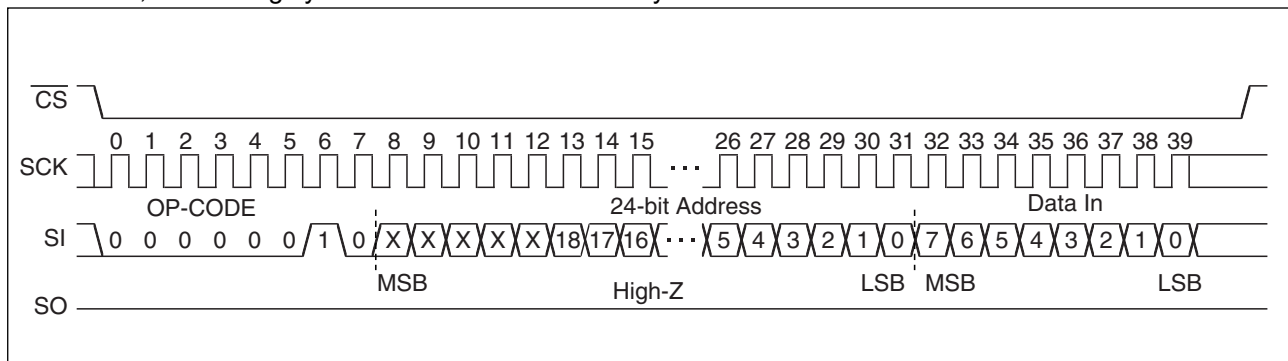
- **READ**

  The READ command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 5-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.
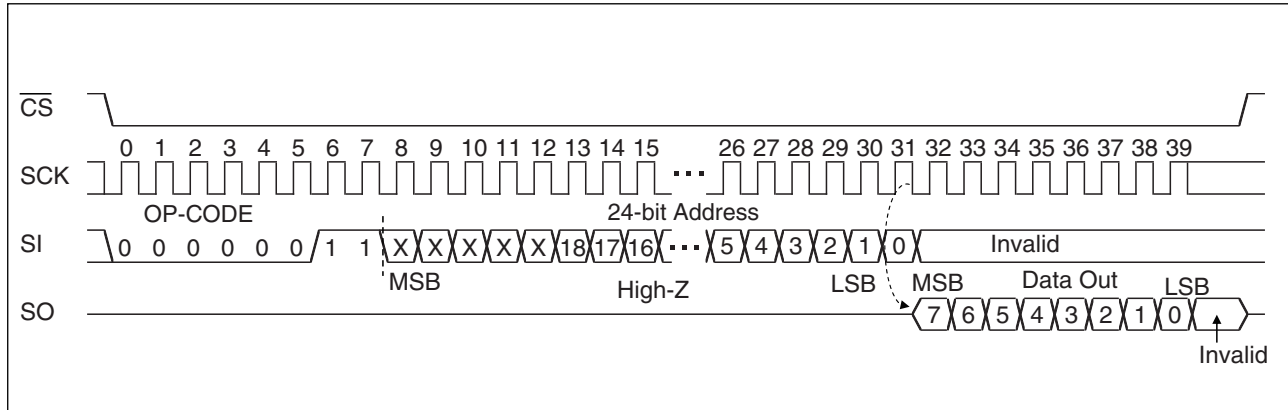

- **WRITE**

  The WRITE command writes data to FeRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 5-bit upper address bit is invalid. When 8 bits of writing data is input, data is written to FeRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before $\overline{CS}$ rising, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued infinitely.
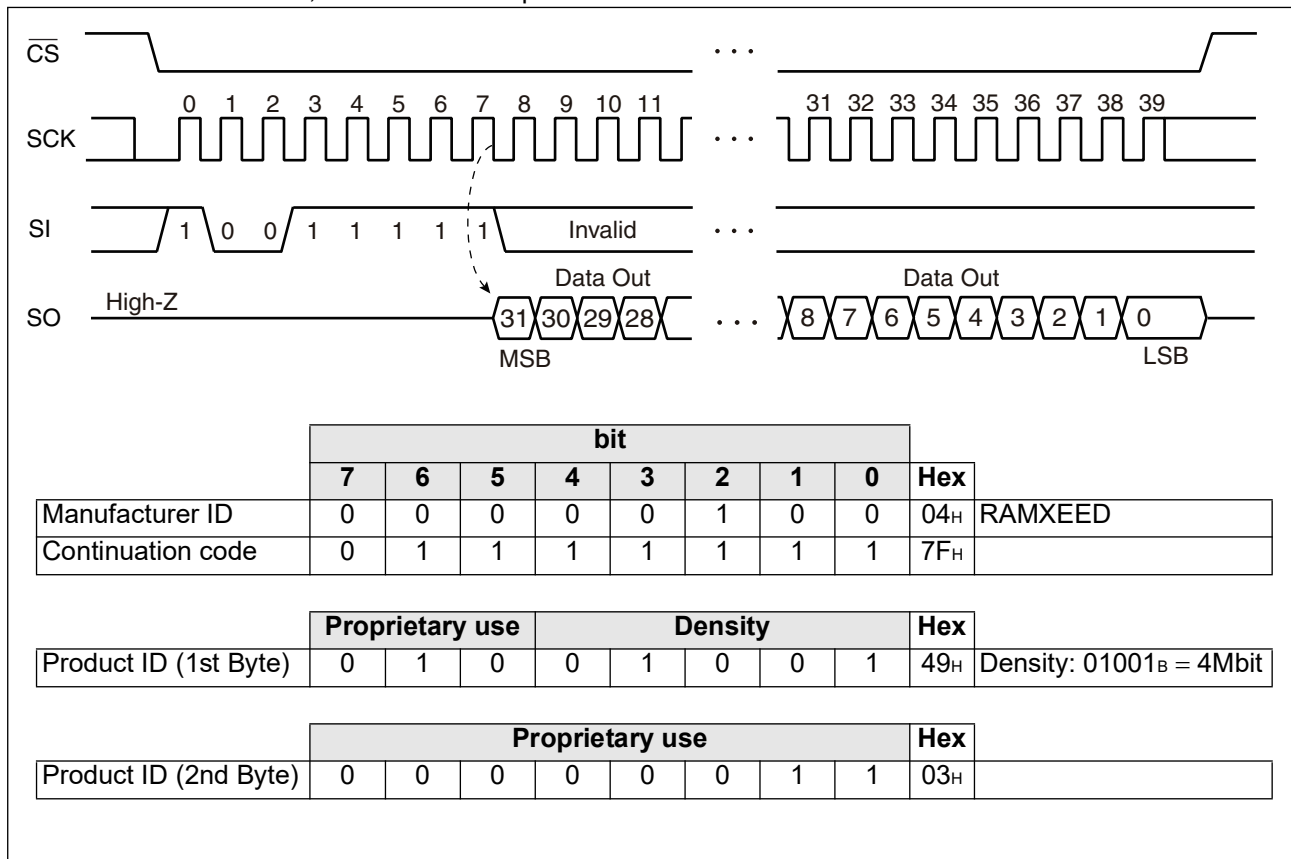
- **FSTRD**

    The FSTRD command reads FeRAM memory cell array data. Arbitrary 24 bits address and op-code of FSTRD are input to SI followed by 8 bits dummy. The 5-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the FSTRD command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.
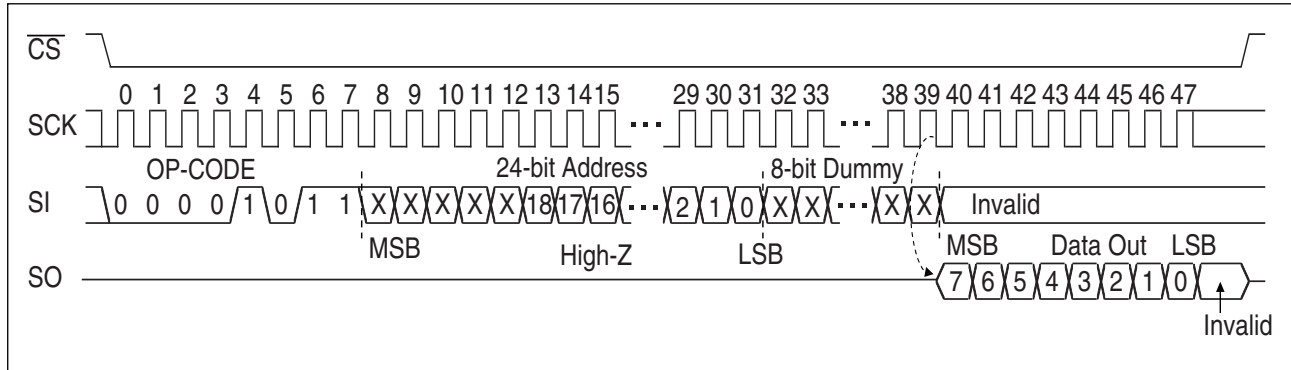

- **RDID**

    The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen.

	bit								Hex	
	7	6	5	4	3	2	1	0		
Manufacturer ID	0	0	0	0	0	1	0	0	04H	RAMXEED
Continuation code	0	1	1	1	1	1	1	1	7FH	

	Proprietary use			Density					Hex	
Product ID (1st Byte)	0	1	0	0	1	0	0	1	49H	Density: 01001B = 4Mbit

|	Proprietary use								Hex	
Product ID (2nd Byte)	0	0	0	0	0	0	1	1	03H	

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- **SLEEP**

The SLEEP command shifts the LSI to a low power mode called "SLEEP mode". The transition to the SLEEP mode is carried out at the rising edge of $\overline{CS}$ after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are ignored and SO changes to a Hi-Z state. If input pin(s) other than $\overline{CS}$ pin is (are) not fixed to VSS or VDD, through current may flow.

Sleep Mode Entry
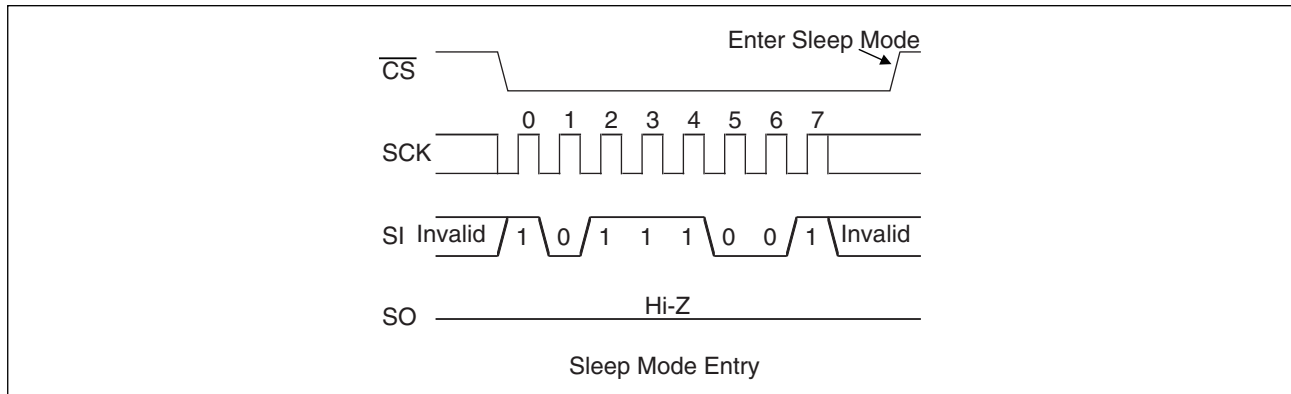
Returning to an normal operation from the SLEEP mode is carried out after t_{REC} (Max 400 μs) time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before t_{REC} time. However, it is prohibited to bring down $\overline{CS}$ to L level again during t_{REC} period.

Sleep Mode Exit

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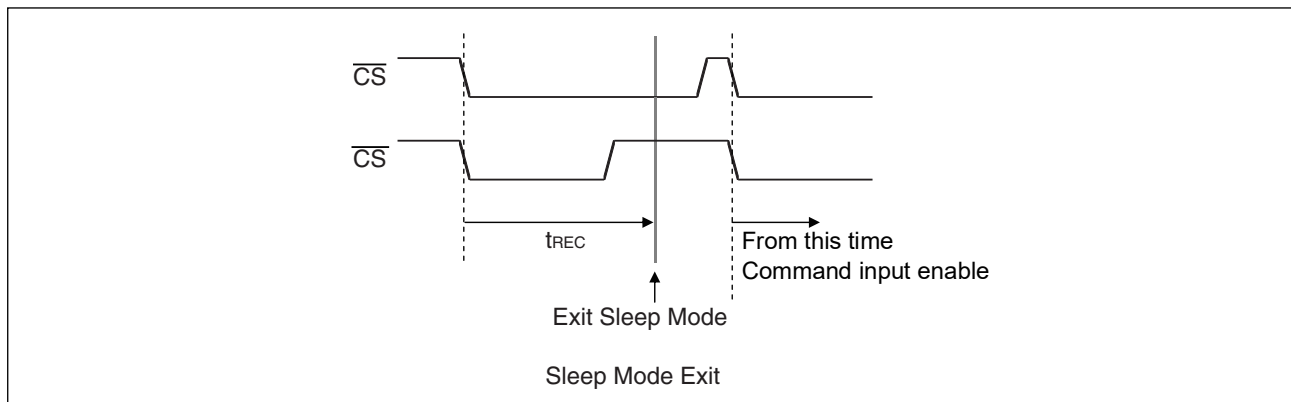
■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

| BP1	BP0	Protected Block
0	0	None
0	1	60000_H to $7FFFF_H$ (upper 1/4)
1	0	40000_H to $7FFFF_H$ (upper 1/2)
1	1	00000_H to $7FFFF_H$ (all)

■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{HOLD}$ is "L" level while $\overline{CS}$ is "L" level. The timing for starting and ending hold status depends on the SCK to be "H" level or "L" level when a $\overline{HOLD}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{HOLD}$ pin transited to "L" level when SCK is "L" level, return the $\overline{HOLD}$ pin to "H" level at SCK being "L" level. In the same manner, in case the $\overline{HOLD}$ pin transited to "L" level when SCK is "H" level, return the $\overline{HOLD}$ pin to "H" level at SCK being "H" level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). If $\overline{CS}$ is rising during hold status, a command is aborted. In case the command is aborted before its recognition, WEL holds the value before transition to hold status.
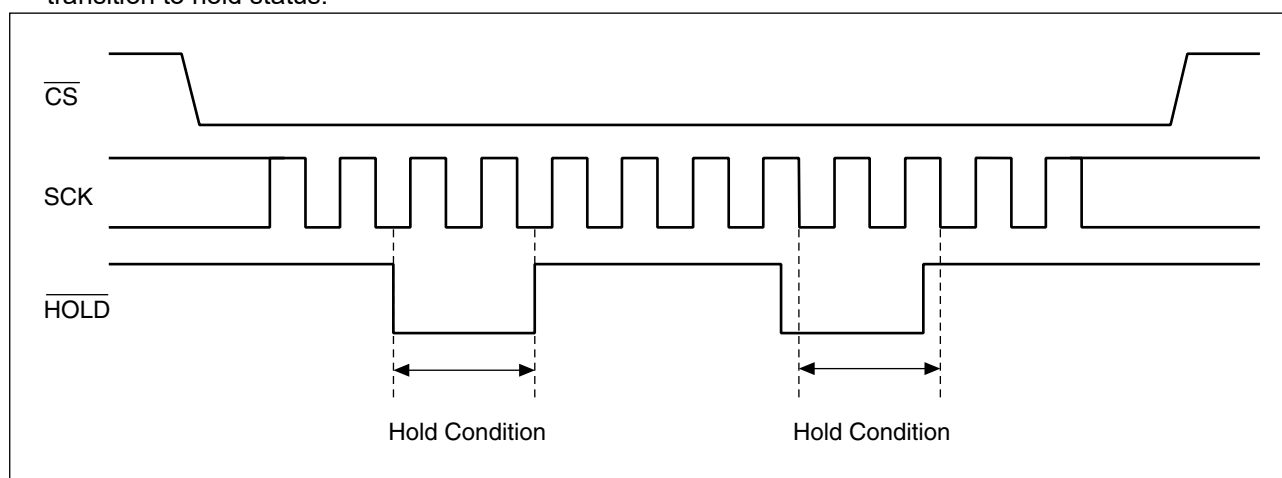
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.0	V
Input voltage*	V_{IN}	− 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Output voltage*	V_{OUT}	− 0.5	$V_{DD} + 0.5 (\leq 4.0)$	V
Operation ambient temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 55	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage[*1]	V_{DD}	1.8	3.3	3.6	V
Operation ambient temperature[*2]	T_A	− 40	—	+ 85	°C

*1: These parameters are based on the condition that V_{SS} is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

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■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current[*1]	$\|I_{LI}\|$	$0 \leq \overline{CS} < V_{DD}$	—	—	200	μA
		$\overline{CS} = V_{DD}$	—	—	1	
		$\overline{WP}, \overline{HOLD}, SCK$ $SI = 0 V$ to V_{DD}	—	—	1	
Output leakage current[*2]	$\|I_{LO}\|$	$SO = 0 V$ to V_{DD}	—	—	1	μA
Operating power supply current	I_{DD}	$SCK = 1MHz$	—	0.15	0.25	mA
		$SCK = 33 MHz$	—	1.5	2.1	
		$SCK = 40 MHz$	—	1.8	2.6	
Standby current	I_{SB}	$SCK = SI = \overline{CS} = V_{DD}$	—	10	50	μA
Sleep current	I_{ZZ}	$\overline{CS} = V_{DD}$ All inputs V_{SS} or V_{DD}	—	5	8	μA
Input high voltage	V_{IH}	$V_{DD} = 1.8 V$ to $3.6 V$	$V_{DD} \times 0.7$	—	$V_{DD} + 0.5$	V
Input low voltage	V_{IL}	$V_{DD} = 1.8 V$ to $3.6 V$	$- 0.5$	—	$V_{DD} \times 0.3$	V
Output high voltage	V_{OH}	$I_{OH} = - 2 mA$	$V_{DD} - 0.5$	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 2 mA$	—	—	0.4	V
Pull up resistance for $\overline{CS}$	R_P	—	18	33	80	kΩ

*1 : Applicable pin : $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, SCK, SI

*2 : Applicable pin : SO

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2. AC Characteristics

Parameter	Symbol	Value				Unit
		V_{DD} = 1.8 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		
		Min	Max	Min	Max	
SCK clock frequency	f_{CK}	0	33	0	40	MHz
Clock high time	t_{CH}	13	—	11	—	ns
Clock low time	t_{CL}	13	—	11	—	ns
Chip select set up time	t_{CSU}	10	—	10	—	ns
Chip select hold time	t_{CSH}	10	—	10	—	ns
Output disable time	t_{OD}	—	12	-	12	ns
Output data valid time	t_{ODV}	—	13	-	9	ns
Output hold time	t_{OH}	0	—	0	—	ns
Deselect time	t_D	40	—	40	—	ns
Data in rising time	t_R	—	50	-	50	ns
Data falling time	t_F	—	50	-	50	ns
Data set up time	t_{SU}	5	—	5	—	ns
Data hold time	t_H	5	—	5	—	ns
HOLD set uptime	t_{HS}	10	—	10	—	ns
HOLD hold time	t_{HH}	10	—	10	—	ns
HOLD output floating time	t_{HZ}	—	20	—	20	ns
HOLD output active time	t_{LZ}	—	20	—	20	ns
SLEEP recovery time	t_{REC}	—	400	—	400	μs

AC Test Condition

Power supply voltage : 1.8 V to 3.6 V
Operation ambient temperature : -40 °C to $+85$ °C
Input voltage magnitude : $V_{DD} \times 0.7 \le V_{IH} \le V_{DD}$
$0 \le V_{IL} \le V_{DD} \times 0.3$

Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

AC Load Equivalent Circuit
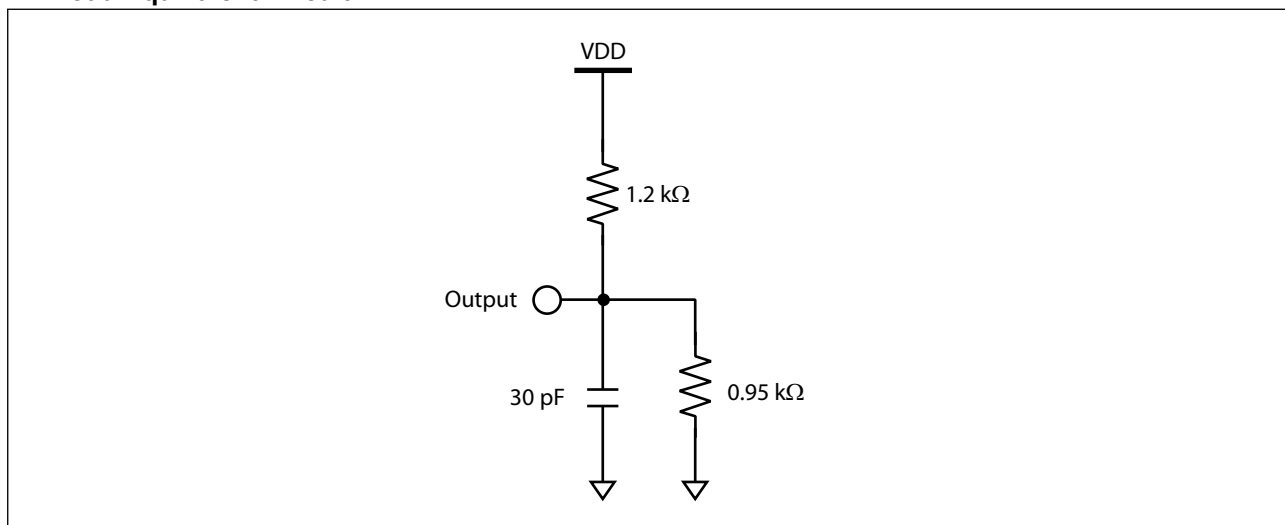
3. Pin Capacitance

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output capacitance	C_O	$V_{DD} = V_{IN} = V_{OUT} = 0$ V,	—	8	pF
Input capacitance	C_I	$f = 1$ MHz, $T_A = +25$ °C	—	6	pF

MB85RS4MT

■ TIMING DIAGRAM

• Serial Data Timing

• Hold Timing

DS501-00053-3v1-E

■ POWER ON/OFF SEQUENCE

* : $\overline{CS}$ (Max) < V_{DD} + 0.5 V
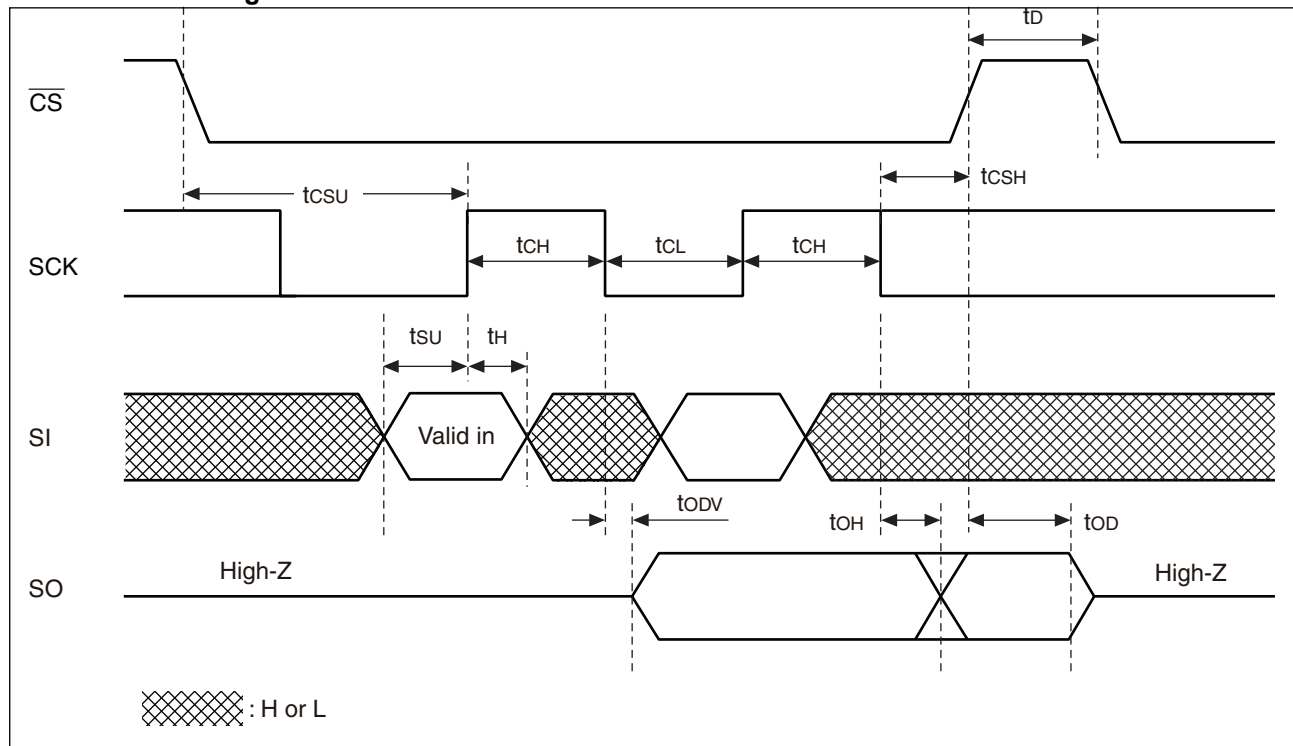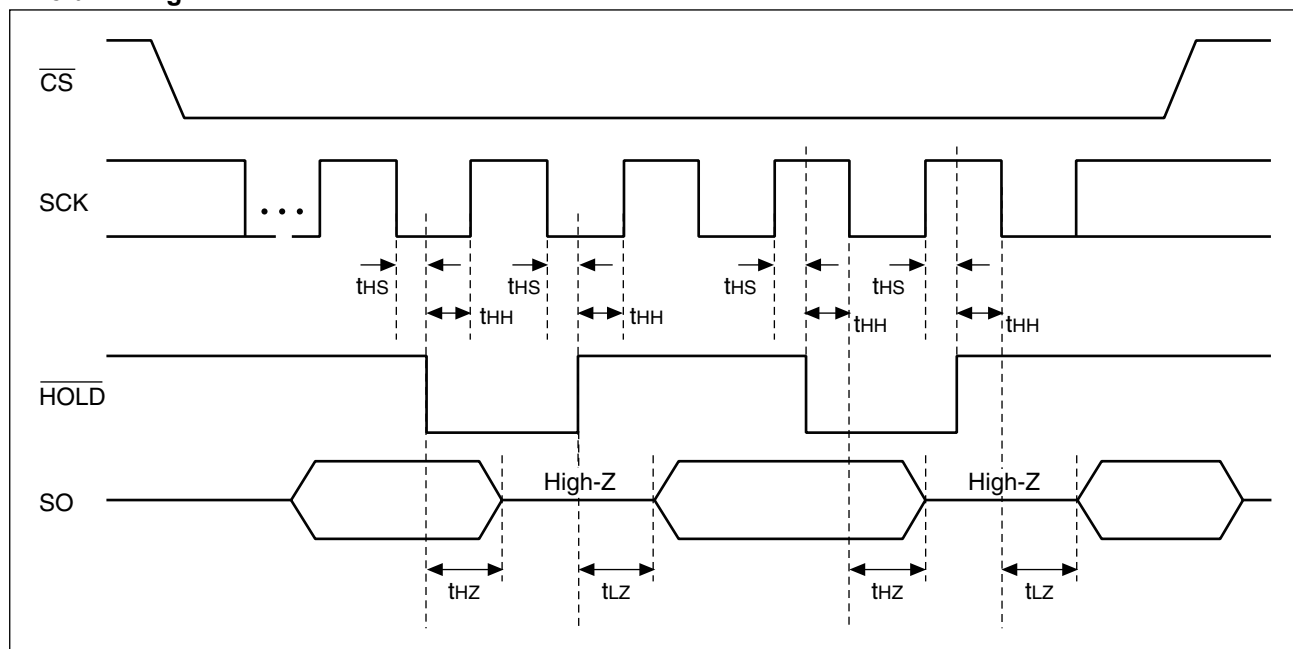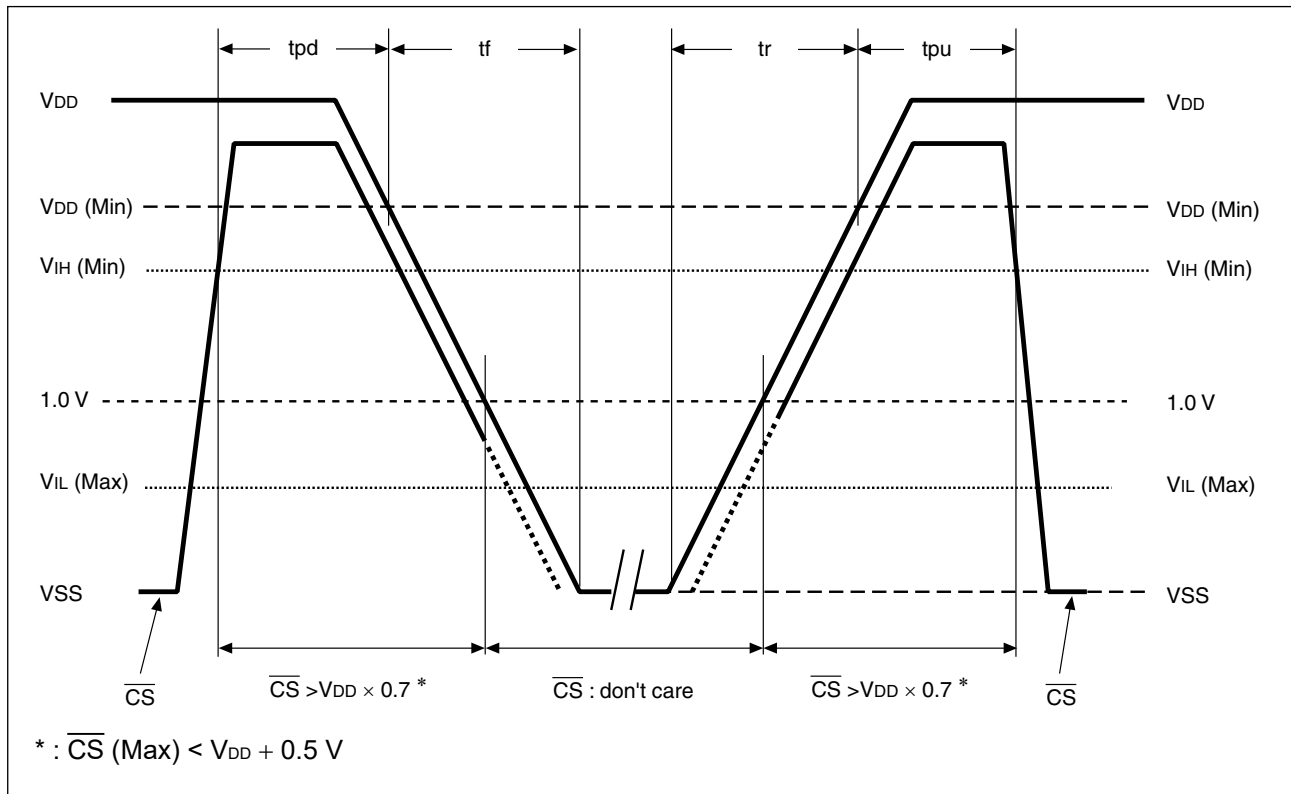
Parameter	Symbol	Value		Unit	condition
		Min	Max		
$\overline{CS}$ level hold time at power OFF	tpd	0	—	ns	VDD=2.7 to 3.6V
		400	—		VDD=1.8 to 2.7V
$\overline{CS}$ level hold time at power ON	tpu	250	—	μs	
Power supply rising time	tr	0.05	—	ms/V	
Power supply falling time	tf	0.1		ms/V	

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

■ FeRAM CHARACTERISTICS

Parameter	Value		Unit	Remarks
	Min	Max		
Read/Write Endurance*1	10^{14}	—	Times	Operation Ambient Temperature $T_A = +85\ °C$ Total number of reading and writing.
Data Retention*2	10	—	Years	Operation Ambient Temperature $T_A = +85\ °C$
	95	—		Operation Ambient Temperature $T_A = +55\ °C$
	≥ 200	—		Operation Ambient Temperature $T_A = +35\ °C$

*1 : For details on the Read/Write endurance value, please refer to "■Read/Write endurance about FeRAM".

*2 : Minimum values define retention time of the first reading/writing data after shipment, and these values are

calculated by qualification results.

■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ Read/Write endurance about FeRAM

The value for Read/Write endurance apply to the total number of read and write operations per row in FeRAM. This is because FeRAM needs writing operation after each reading operations.Each row in the memory array has 32 internal outputs, and 8 outputs are selected by A0 and A1. In continuous Read/Write operations, after selecting a certain address and automatically incrementing until A0 and A1 change from (0,0) to (1,1), the Read/Write count endurance count is totaled as one operation. Subsequently, when incrementing automatically and switching to the next row, each row is counted as a new Read/Write operation. If /CS is raised and then the same row is selected again, it is counted as the second operation for that row.

As an actual usage example, if you loop through and access only a memory area (64 bytes or 256 bytes) specified by a specific address in the entire memory area, the number of years it will take to reach 10^{14} times is as below.

As shown here, with a write endurance of 10^{14} times, even in extreme cases there is enough time before the upper limit is reached, and under normal conditions of use it can be used without worrying about the number of writes/reads.

Operating frequency	Years reached when looping continuously through 64 byte area	Years reached when looping continuously through 256 byte area
40MHz	42.6	164
20MHz	85.1	328
10MHz	170.0	657

■ ESD AND LATCH-UP

Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant		$\geq |2000\ V|$
ESD CDM (Charged Device Model) JESD22-C101 compliant	MB85RS4MTPF-G-BCE1 MB85RS4MTPF-G-BCERE1	$\geq |1000\ V|$
Latch-Up (C-V Method) Proprietary method		$\geq |200\ V|$

• C-V method of Latch-Up Resistance Test
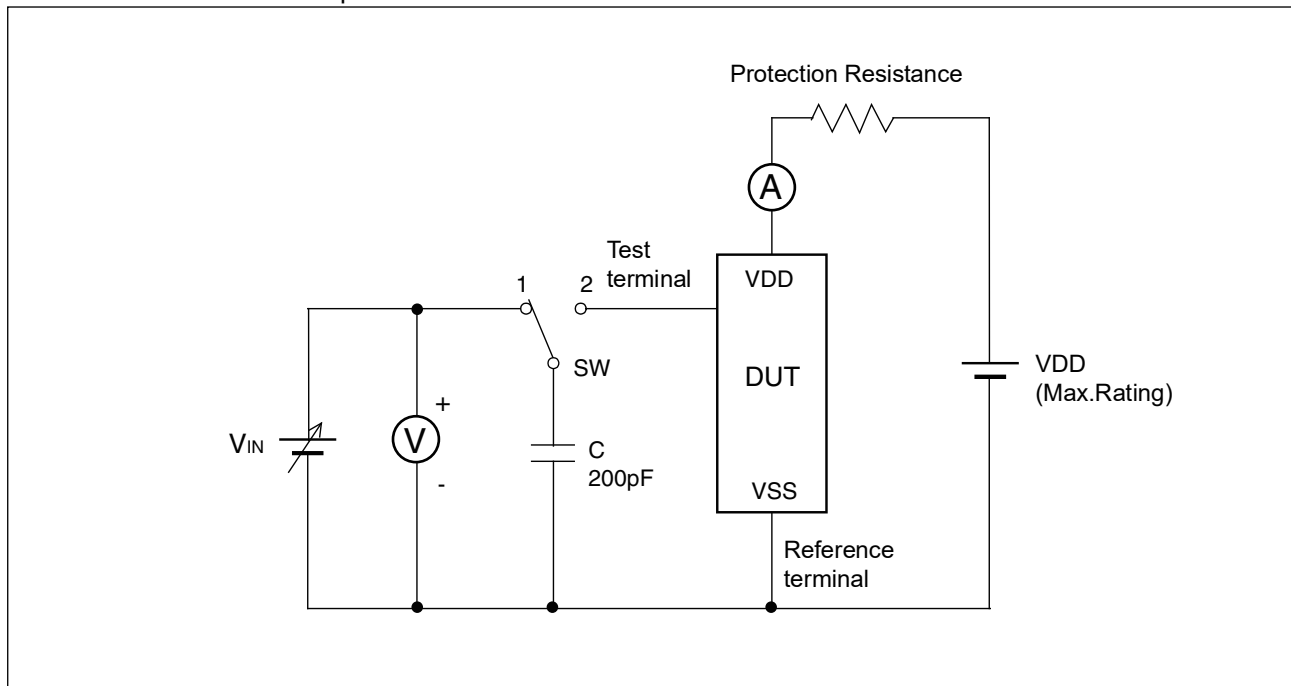
Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.
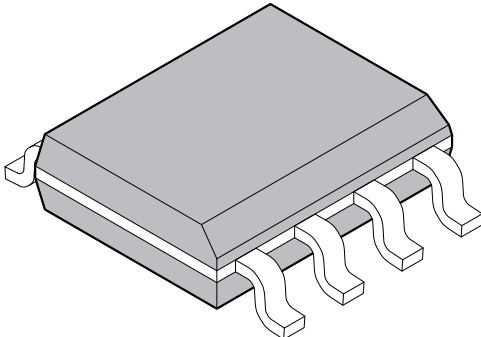
■ ORDERING INFORMATION :

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS4MTPF-G-BCE1	8-pin plastic SOP (208mil)	Tube	— *
MB85RS4MTPF-G-BCERE1	8-pin plastic SOP (208mil)	Embossed Carrier tape	500

* : Please contact our sales office about minimum shipping quantity.

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■ PACKAGE DIMENSIONS

MB85RS4MTPF-G-BCE1/MB85RS4MTPF-G-BCERE1

8-pin plastic SOP (208mil)		
Lead pitch	1.27 mm	
Package width × package length	5.30 mm × 5.65 mm	
Lead shape	Gullwing	
Sealing method	Plastic mold	
Mounting heigth	1.73 mm MAX	

8-pin plastic SOP (208mil)

Note *: These dimensions do not include resin protrution.
Pins width not do ninclude tie bar cutting remaindar.

8pin   5pin

1pin   4pin

1.27 BSC.   0.42±0.10

$5.30±0.10^*$

$8.10±0.10$

5.65±0.10*

(1.50)

1.73(Max)

0.10 S

"F"

0.10(Min)

0.20〜0.25

0.40(Min)

Details of "F" part

Dimenssion in mm

■ MARKING (Example)

[MB85RS4MTPF-G-BCE1]
[MB85RS4MTPF-G-BCERE1]

RS4MT
11900
V00

[8-pin plastic SOP 208mil]

S4MT: Product name
11900: 1(CS code) + 1900(Year and Week code)
V00: Trace code

■ PACKING INFORMATION
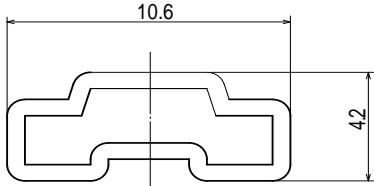
1. Tube (MB85RS4MTPF-G-BCE1)

1.1 Tube Dimensions
• Tube/stopper shape (example)

Tube

Stopper
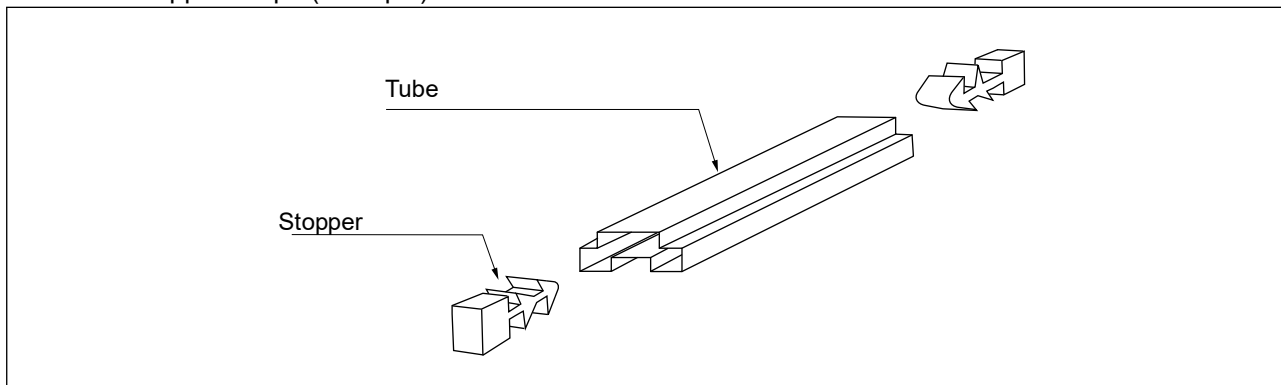
• **Tube cross-sections and Maximum quantity**

Maximum quantity		
pcs/tube	pcs/inner box	pcs/outer box
80	4,000 (50 tube/inner box)	16,000 (Max:4 inner box/ outer box)

10.6

4.2

tube length: 508

No heat resistance.
Package should not be baked by using tube.

(Dimensions in mm)

• **Direction of index in tube**

Index mark

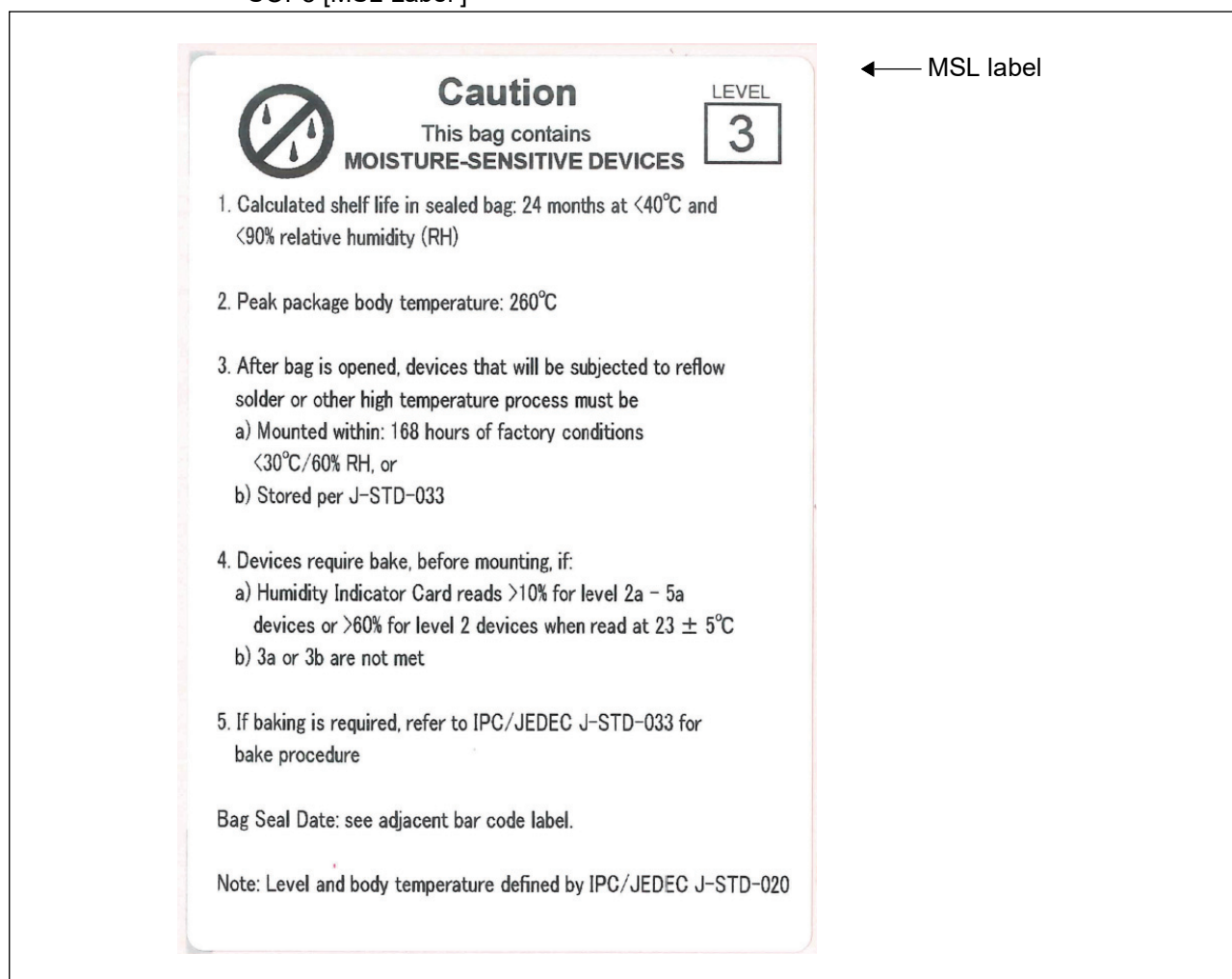## 1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)

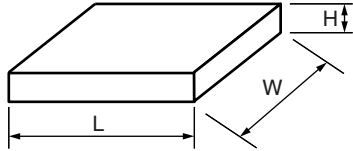[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXX (Part number)	
☐G ⊘Pb	← C-3 Label
(3N)1 XXXXXXXXXXXXXX XXX (LEAD FREE mark)	
▌▌▌▌▌▌▌▌▌ (Part number and quantity)	
QC PASS	
(3N)2 XXXXXXXXXX XXXXXX	
▌▌▌▌▌▌▌▌▌ (Control number bar code)	
XXX pcs (Quantity)	
XXXXXXXXXXXXXX (Part number)	
▌▌▌▌▌▌▌▌▌▌▌ (Part number bar code)	
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx	← Perforated line
XXXXXXXXXXXXXX (Part number)	← Supplemental Label
(Control number bar code)	
▌▌▌▌▌▌▌ XX/XX XXXX-XXX XXX	
(Package count) XXXX-XXX XXX	
XXXXXXXXXX (Control number) (Lot Number and quantity)	
XXXXXXXXXXXXXX (Comment)	

1.3 Dimensions for Containers

(1) Dimensions for inner box

L	W	H
540	125	75

(Dimensions in mm)

(2) Dimensions for outer box

L	W	H
565	270	180
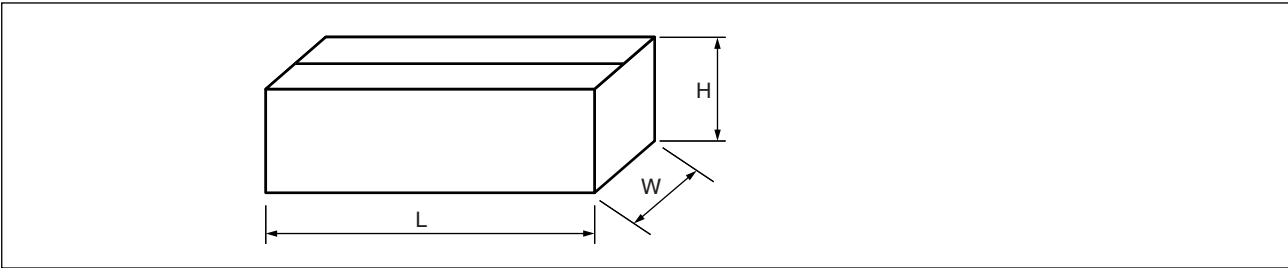
(Dimensions in mm)

2. Emboss Tape (MB85RS4MTPF-G-BCERE1)

2.1 Tape Dimensions (not drawn to scale)(8-pin plastic SOP 208mil)

Maximum storage capacity		
pcs/reel(φ254mm)	pcs/inner box	pcs/outer box
500	500 (1 pack/inner box)	3,000 (6 inner boxes/outer box:Max.)

SEC.B-B

SEC.A-A

(Dimensions in mm)

Heat proof temperature : No heat resistance.

Package should not be baked by using tape and reel.

2.2 IC orientation

• example

Index mark

(User Direction of Feed)   (Reel side)   (User Direction of Feed)

2.3 Reel dimensions

Reel cutout dimensions

W1

W2
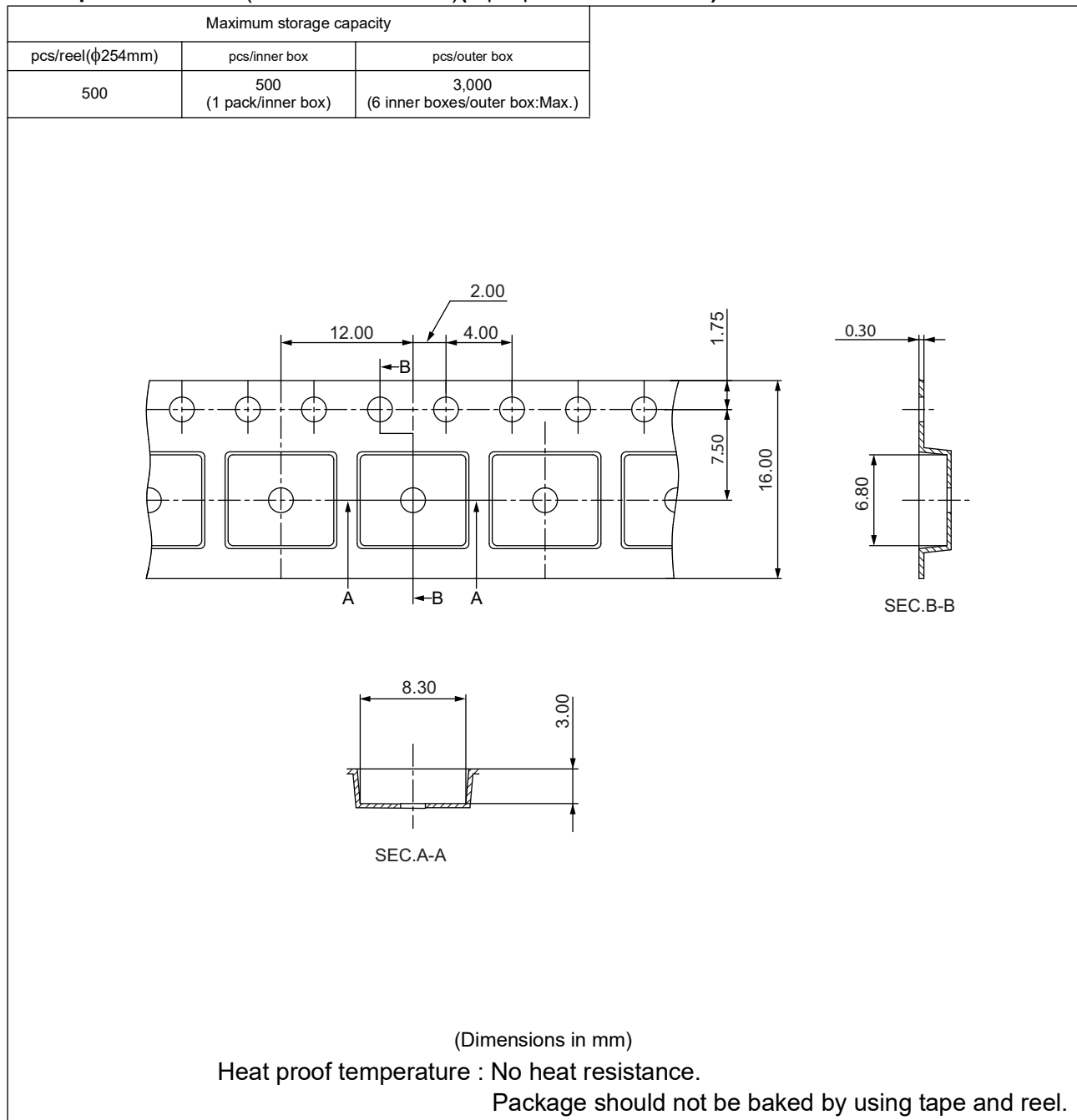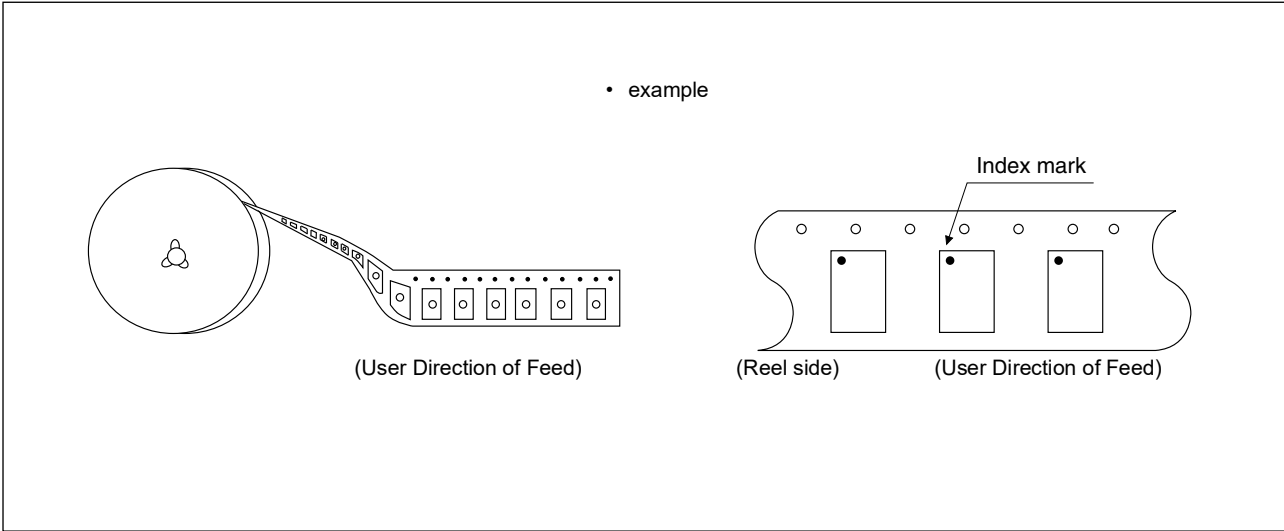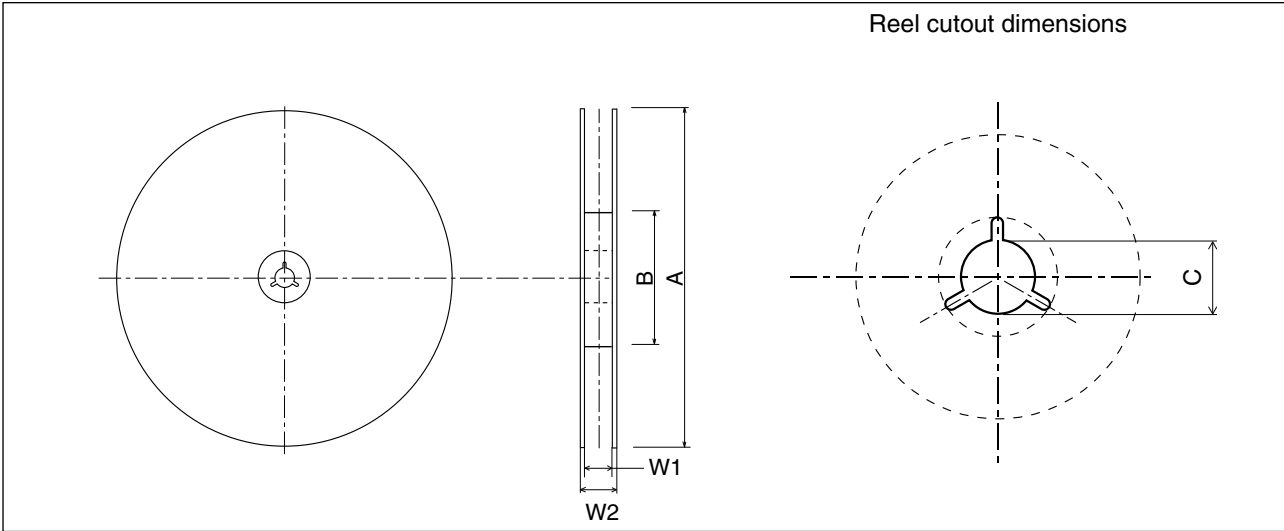
Dimensions in mm

A	B	C	W1	W2
254	100	13	17.5	21.5

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2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]

XXXXXXXXXXXXXX   (Part number)

[G] (Pb)   ← C-3 Label

(3N)1 XXXXXXXXXXXXXX   XXX   (LEAD FREE mark)
(Part number and quantity)
QC PASS

(3N)2 XXXXXXXXXX   XXXXXX
(Control number bar code)

XXX pcs   (Quantity)
XXXXXXXXXXXXXX   (Part number)

(Part number bar code)

XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx   ← Perforated line

XXXXXXXXXXXXXX   (Part number)   ← Supplemental Label
(Control number bar code)
XX/XX   XXXX-XXX   XXX
(Package count)   XXXX-XXX   XXX
XXXXXXXXXX   (Control number)   (Lot Number and quantity)
XXXXXXXXXXXXXX   (Comment)
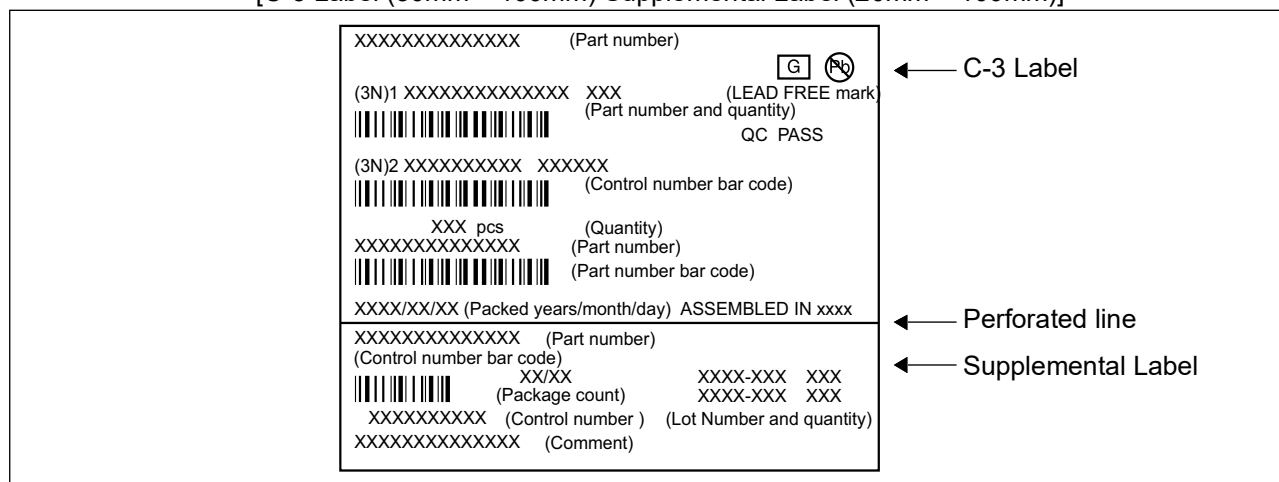
Label II: Moisture Barrier Bag (It sticks it on the Aluminum laminated bag)
SOP8 [MSL Label]

← MSL label

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
3

1. Calculated shelf life in sealed bag: 24 months at <40°C and <90% relative humidity (RH)

2. Peak package body temperature: 260°C

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: 168 hours of factory conditions <30°C/60% RH, or
   b) Stored per J–STD–033

4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads >10% for level 2a – 5a devices or >60% for level 2 devices when read at 23 ± 5°C
   b) 3a or 3b are not met

5. If baking is required, refer to IPC/JEDEC J–STD–033 for bake procedure

Bag Seal Date: see adjacent bar code label.

Note: Level and body temperature defined by IPC/JEDEC J–STD–020

2.5 Dimensions for Containers

(1) Dimensions for inner box

Tape width	L	W	H
12	265	260	50

(Dimensions in mm)

(2) Dimensions for outer box

L	W	H
565	270	180

(Dimensions in mm)

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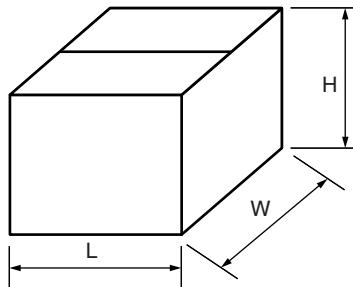
■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn left side of that page.

Page	Section	Change Results
1,17	High endurance	10^{13}times/byte → 10^{14}times
18	Read/Write endurance about FeRAM	Add information

RAMXEED LIMITED

Shin-Yokohama Chuo Building, 2-100-45 Shin-Yokohama,

Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan

https://ramxeed.com/